TQ components

TQM 8xxL
Hardware - Manual

Revision 201

2000-12-20

Hardware Manual for:

TQM823L	Rev. 100
	Rev. 200
	Rev.300
TQM850L	Rev. 100
	Rev. 200
	Rev.300
TQM855L	Rev.200
	Rev.300
TQM860L	Rev. 100
	Rev. 200
	Rev.300

Contents

1 Introduction

Top Quality embedded Microcontroller Systems

High integration and high reliability are what set the TQ-Components industrial microcontroller modules apart from the rest. TQ-Components Minimodules from credit-card to half credit-card size are unbeatable in various applications. With an ever-expanding product line and clear technology migration path, TQ-Components offers OEMs uncompromising excellence in microcontroller modules. In a variety of industrial measurement, process regulation and control developments engineers confronted with the task of developing a complex monitoring / control system under time constraints are the prime beneficiaries of our microcontroller devices. Compare the advantage of the implementing a TQ-Components module to the total cost of a completely new circuitry design.

Time to market

TQ-Components microcontroller modules provide a drop-in CPU solution, with complete CPU kernel functionality on board. This enables engineers to take a project from concept to prototype or market in weeks, rather than in months or longer.

Reliability

TQ-Components modular embedded microcontroller Minimodules have proven to be reliable and rugged in numerous demanding and critical applications. Our highly knowledgeable team of electronic engineers has wide experience in designing embedded microcontroller Modules. The team's commitment to quality and reliability is evident throughout the whole TQ-Components product line.

Upgrade ability

Thanks to the flexibility of TQ's product architectures, you will be able to enhance your products by taking advantage of a new technology when it becomes available. Our products offer a migration path so you can upgrade features or performance without major redesign.

TQ-Minimodules offers you ...

Best price-performance relationship

uncompromising use of most modern production - technology
low price through high production quantity
Customised versions on requests

Maximum performance on small footprint

double-sided SMT technology
fine pitch multilayer printed circuit boards
using latest chip technology
using latest Flash memory technology

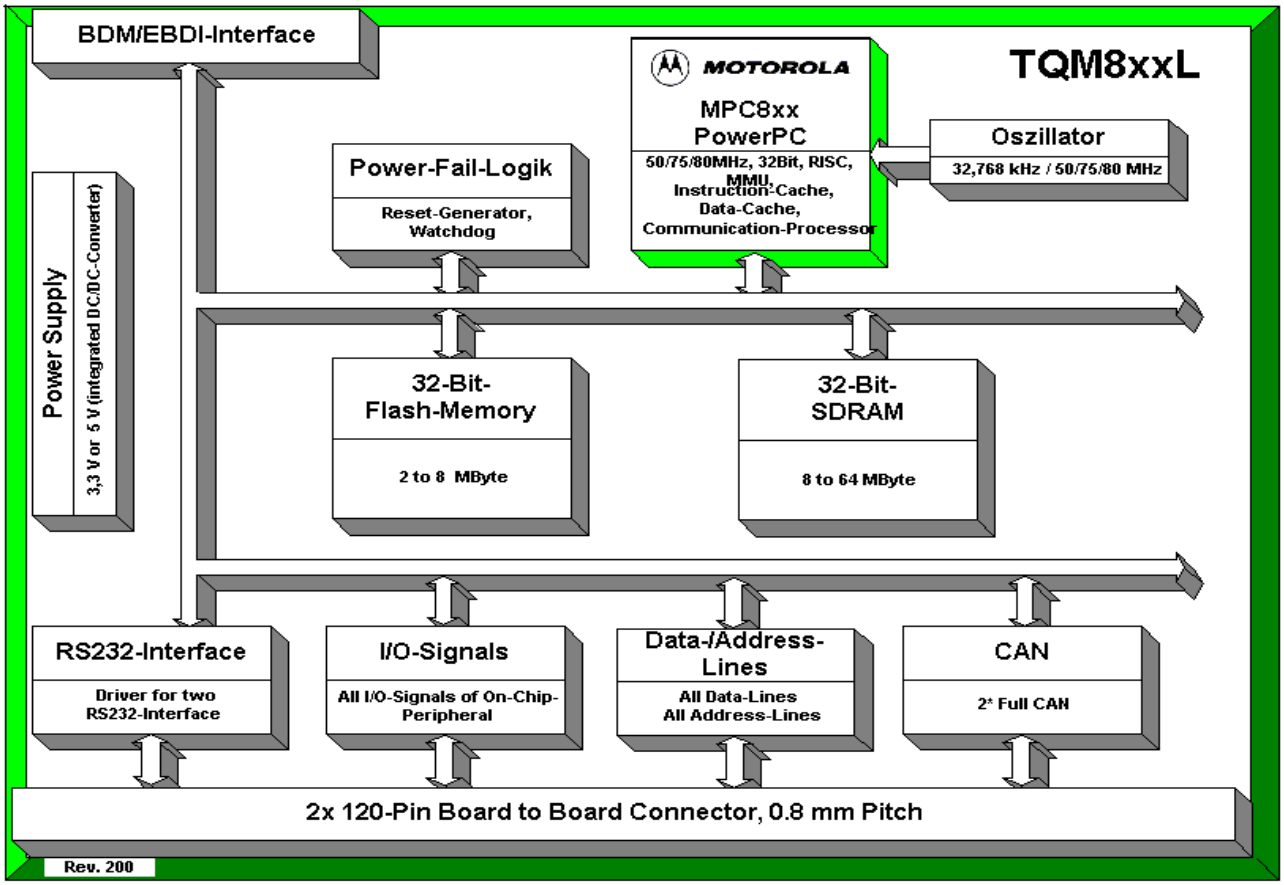
save time and money in your development

complete CPU kernel functionality on board
immediate start with particular monitor-program
works with most modern software development tools such as compilers and debuggers
design-in support through the manufacturer

save time and money in your production and service

Download-Function for development, production and service
simple Firmware-Updates by download-function
Download via Standard RS232-Interface without additional switches and jumpers
service-friendly modular construction

2 Block Diagram



2.1 32-Bit Microprocessor

32-Bit-PowerPC-RISC-CPU, 50MHz Clock Frequency
32-Bit-Core with variable Instruction-Pipeline and Branch-Prediction Precise Exception Model
26/32 Address Lines, 4 GByte max. Memory Size
Instruction-Cache
Data-Cache
4-times Write- and Read-Buffer, Burst-Access
2 chanel DMA controller (8/16Bit), 32 universal 32 bit register, debugging support
external clock frequency 50 MHz
4 GB logical and physical memory size
memory management unit with translation lookaside buffer (TLB) for data and code
memory management unit supports multiple Page Size, 16 Virtual Address SpacesandProtectionGroups
Communication Processor Module - Integrated RISC-Controller to set I/O-Functions

Details see Motorola MPC823 / MPC850 / MPC855 / MPC860 User's Manual

2.2 Memory

2.2.1 Flash

1 or 2 memory banks

2 to 8 MByte
32-Bit memory
On-Board-programmable (Bootloader for Flash-Programming via serial interface)
Standard: 4 MByte, 90 ns (4 Waitstates)

2.2.2 SDRAM

synchronous dynamic RAM (SDRAM)

4 to 64 MByte (4, 16, 32, 64 MByte)
one Memory Bank with 32-Bit memory
external expandable with PS/2-Moduls (additional external Busdriver necessary)
Standard: 16 MB, 100 Mhz, Access Time 3 + 2 (Single read)
2 + 1 + 1 + 1 + 2 (Burst read)
3 + 2 (Single write)
2 + 1 + 1 + 1 + 2 (Burst write)

2.3 Reset - Logic

Double Voltage Control (1x 3,3, 1x 5 V)

external Reset-Input
MAX816TCSA

2.4 Interface

2.4.1 Serial - Interface

max. 115200 Baud

Short-Circuit protected RS232-Driver for 2 UARTs
all Signals also available without drivers
Standard: Driver for 2x RxD/TxD^

2.4.2 Bus - Interface

26 / 32 Bit Address- and 32 Bit Data-Bus

8-, 16- and 32-Bit-Access
Timing programmable
DMA or CPU-Access
All I/O- and Control-Lines available

2.4.3 CAN - Interface

2 CAN Controllers Intel 82527

Using Interrupt Request 4 (IRQ4#)
Using Chip Select 3 (CS3#)

2.4.4 EBDI / BDM Interface

All Lines of Motorola EBDI (Enhanced Background Debugging Interface)
direct access on all registers and memories

2.4.5 Other Interfaces

Microprocessor dependent
Ethernet / Fast Ethernet
ATM
USB
Multi HDLC
PCMCIA
I²C
LCD
Video

2.5 Info LED

The LED installed on the top of the module is connected to the reset pin SRESET# of the CPU. It lights when SRESET# is active.

2.6 Power Supply

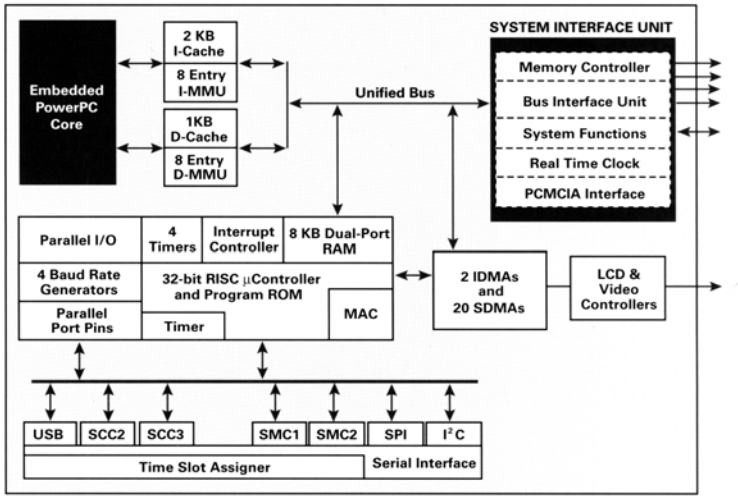
3.3V Power Supply (Direct Input)

5.0V Power Supply (5.0V to 3.3V integrated DC/DC Converter)

3 Microprocessor

3.1 MPC823/823e

The MPC823e microprocessor is a versatile, one-chip integrated microprocessor and peripheral combination that can be used in a variety of portable electronic products. It is a low-cost version of the MPC823 microprocessor, except it has been enhanced with additional communication and display capabilities. Specifically, it supports the universal serial bus and video display systems and the existing LCD interface on the MPC823 device. The MPC823e microprocessor particularly excels in low-power, portable, image capture, and personal communication products. It integrates a high-performance embedded PowerPC ™ core with a communication processor module that uses a specialised RISC processor for imaging and communication. The communication processor module can perform embedded signal processing functions for image compression and decompression and supports seven serial channels—two serial communication controllers, two serial management controllers, one I²C port, one universal serial bus channel, and one serial peripheral interface. This two processor architecture consumes power more efficiently than traditional architectures because the communication processor module frees the core from peripheral responsibilities like imaging and communication.



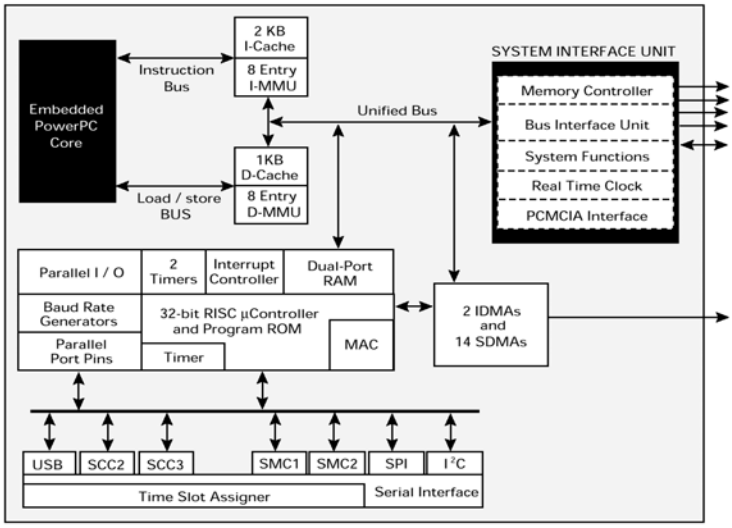
The following list summarises the main features of the MPC823 / MPC823e:

Embedded PowerPC Core Provides 99MIPS (Using Dhrystone 2.1) or 172K Dhrystones 2.1 at 75MHz
8K Data Cache and 16K Instruction Cache
Memory Management Units Support Multiple Page Sizes of 4K, 16K, 512K and 8M
Data Bus Dynamic Bus Sizing for 8-,16-, and 32-Bit Buses
twenty-six External Address Lines
Completely Static Design (0–81MHz Operation)
Communication Processor Module
16 x 16-Bit Multiply Accumulate (MAC) Hardware for DSP Functions
Four Independent Baud Rate Generators and Two Input Clock Pins for Supplying Clocks to the SCC and SMC Serial Channels
Two Serial Communication Controllers
Ethernet/IEEE 802.3 Support (10Mbps and Full-Duplex Operation)
Serial Infrared (IrDA) Supporting a Maximum of 4Mbps (SCC2 only)
One Dedicated High-Speed Serial Channel for the Universal Serial Bus (USB)
One SPI ® (Microwire-Compatible) Interface that Supports Master and Slave Modes
One I²C (Inter-Integrated Circuit) Port
Video/LCD Controller supports Digital TFT LCD Panels and Analog NTSC/PAL Displays
Single-Socket PCMCIA-ATA Interface, Master Interface, Release 2.1-Compliant
EEE 1149.1 Test Access Port (JTAG)
Advanced On-Chip Emulation Debug Mode
Low Power Support
3.3V Operation with 5V TTL Compatibility for the JTAG and Communication Processor Module Port Pins and 3.3V for All Others.

Details see Motorola MPC823/823e Product Brief and MPC823/823e User's Manual

3.2 MPC850

The MPC850 microprocessor is a versatile, one-chip integrated microprocessor and peripheral combination that can be used in a variety of portable electronic products. In addition, its lower cost implementation of the MPC860 provides an effective price/performance solution for Networking and Communication applications. The MPC850 is powered by a high-performance embedded PowerPC core and include extensive communications and system integration support, simplifying the development effort and decreasing time-to-market. An example of the integration that the MPC850 provides begins with the communication processor module (CPM) with offloads tasks from the embedded PowerPC core providing increased performance and efficiency over more traditional CPU architectures. Furthermore, the CPM of the MPC850 supports up to seven serial channels, two serial communication controllers (SCC's), one I²C port, one universal serial bus channel (USB), including two serial management controllers (SMC's), and one serial peripheral interface (SP).

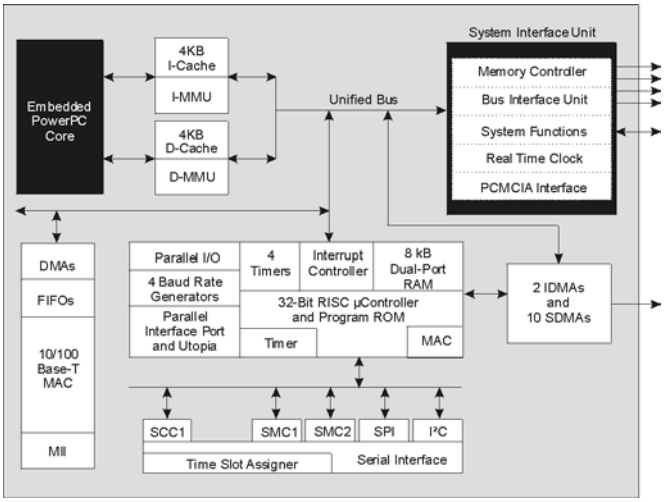


The following list summarises the main features of the MPC850:

Embedded PowerPC Core with 87 MIPS at 66 MHz (using Dhrystone 2.1)
2 Kb Instruction Cache
1 Kb Data Cache
Instruction and Data MMUs
Up to 32-Bit Data Bus (Dynamic Bus Sizing for 8, 16, and 32 Bits)
26 External Address Lines
Complete Static Design (0-66 MHz Operation)
Memory Controller (Eight Banks)
System Integration Unit (SIU)
Communications Processor Module (CPM)
Four Baud Rate Generators
Up to two SCC's (Serial Communication Controller with Ethernet Support)
One USB Port
Two SMC's (Serial Management Channels)
One SPI (Serial Peripheral Interface)
One I²C (Inter-Integrated Circuit) Port
Parallel Interface Port (supports UTOPIA)
PCMCIA Interface
Low Power Support
Debug Interface
3.3V Operation with 5V TTL Compatibility for the JTAG and Communication Processor Module Port Pins and 3.3V for All Others.

3.3 MPC855

The MPC855 communications controller is a member of the MPC8xx family targeted at cost sensitive general purpose networking controller applications. The MPC855T can be used in a variety of controller applications, excelling particularly in low cost communications and networking products, such as SOHO routers, ADSL, and cable modems.The MPC855 integrates three separate processing blocks. The first two, common with all MPC8xx devices, are a high-performance PowerPC[a] core, which is used as a general-purpose processor for application programming and a RISC communications processor embedded in the communications processor module (CPM). The third block is a 10/100-Mbps Fast Ethernet controller with integrated FIFOs and bursting DMA. Additionally, since the CPM of the MPC855T is based on the CPM of other MPC8xx devices, support for ATM, HDLC, and the QMC (QUICC multichannel controller) multichannel protocol is also provided. This support for multichannel protocol processing, ATM and 10/100-Mbps Ethernet in one chip makes the MPC855T idealfor cost sensitive networking and telecommunications systems.



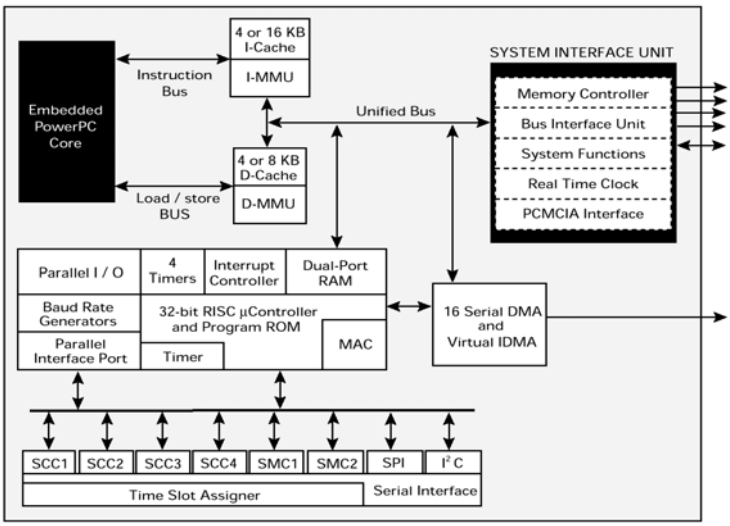
The following list summarises the key MPC860 PowerQUICC features:

Embedded PowerPC Core with 106 MIPS at 80 MHz (using Dhrystone 2.1)
4 Kbyte Data Cache and 4 Kbyte Instruction Cache, Each with an MMU
Up to 32-Bit Data Bus (Dynamic Bus Sizing for 8,16, and 32 Bits)
32 Address Lines
Complete Static Design (0–80 MHz Operation)
Memory Controller (Eight Banks)
Variable Block Sizes, 32 Kb to 256MB
System Integration Unit (SIU)
IEEE 1149.1 Test Access Port (JTAG)
Communications Processor Module (CPM)
On Chip 16x16 Multiply Accumulate Controller (MAC)
One Baud Rate Generators
One SCC (Serial Communication Controller)
Ethernet/IEEE 802.3 Optional on SCC1-4, Supporting Full 10-Mbps Operation
Serial Infrared (IrDA)
Two SMC's (Serial Management Channels)
One SPI (Serial Peripheral Interface)
One I²C (Inter-Integrated Circuit) Port
Parallel Interface Port (Centronics 1 Interface Support)
PCMCIA Interface, Release 2.1 Compliant
Low Power Support
Advanced On-Chip-Emulation Debug Mode
3.3V Operation with 5V TTL Compatibility

Details see Motorola MPC855 Product Brief and MPC855 User's Manual

3.4 MPC860

The MPC860 PowerQUICC is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications, excelling particularly in communications and networking products. The PowerQUICC can be described as a next-generation MC68360 QUICC for network and data communication applications, providing higher performance in all areas of device operation including flexibility, extensions in capability, and integration. The MPC860 PowerQUICC, like the MC68360 QUICC integrates two processing blocks. One block is the Embedded PowerPC Core and the second block is a Communication Processor Module (CPM) that closely resembles the MC68360 CPM. The CPM supports four serial communications controllers (SCCs) on the device; however, there are actually eight serial channels: four SCCs, two serial management controllers (SMC's), one serial peripheral interface (SPI) and one I 2 C interface. This dual-processor architecture provides lower power consumption than traditional architectures because the CPM off-loads peripheral tasks from the Embedded PowerPC



The following list summarises the key MPC860 PowerQUICC features:

Embedded PowerPC Core with 88 MIPS at 66 MHz (using Dhrystone 2.1)
4 Kbyte Data Cache and 4 Kbyte Instruction Cache, Each with an MMU
Up to 32-Bit Data Bus (Dynamic Bus Sizing for 8,16, and 32 Bits)
32 Address Lines
Complete Static Design (0–80 MHz Operation)
Memory Controller (Eight Banks)
Variable Block Sizes, 32 Kb to 256MB
System Integration Unit (SIU)
IEEE 1149.1 Test Access Port (JTAG)
Communications Processor Module (CPM)
On Chip 16x16 Multiply Accumulate Controller (MAC)
Four Baud Rate Generators
Four SCCs (Serial Communication Controllers)
Ethernet/IEEE 802.3 Optional on SCC1-4, Supporting Full 10-Mbps Operation
Serial Infrared (IrDA)
Two SMC's (Serial Management Channels)
One SPI (Serial Peripheral Interface)
One I²C (Inter-Integrated Circuit) Port
Parallel Interface Port (Centronics 1 Interface Support)
PCMCIA Interface, Release 2.1 Compliant
Low Power Support
Advanced On-Chip-Emulation Debug Mode
3.3V Operation with 5V TTL Compatibility

Details see Motorola MPC860 Product Brief and MPC860 User's Manual

4 Memory

The following section describes the used memory on the Minimodule for efficient use.

4.1 General Function

The installed processor is equipped with 8 freely programmable chip select outputs which access the respective system components. For each Memory Bank of one Chip Select Output a flexible Bus configuration can be used. This include Bus type, Bus width, Timing, Write Protection and others.

The Bus-Timing can be set-up in two ways:

Access via the General Purpose Chip-Select Machine GPCM
Access via one or two User-Programmable Machines UPBA / UPMB

The GPCM allows the access to many Memory Chips and other I/O-Devices with a SRAM like Interface. The principle of the access is always similar, Set-up- and Hold-Timing and the complete access time (wait states) can be set-up. Both Chip Select and the Control signals OE# and WE[0:3]# will be generated by the GPCM.

Details see MPC8xx User's Manual.

TheGPCM set the CS0# Signal as Boot Chip Select. The Reset configuration enables the Microprocessor to read from Bank 0 at lowest Access Time and Buswidth, which is Reset Value.

The UPM's are more flexible to use different Bus-Timings. Besides the chip select, the UPM can set the Byte-Select-Signals [BS80:3]# and up to six Output Signals (GPL_A[0:5] and GPL_B[0:5]) with maximum resolution of 1/4 CLKOUT-Period. GPL_A4 and GPL_B4 can be configured as UPWAITA or UPWAITB Wait Signal. The Set-up of the signals will use Set-up-Tables within the internal RAM. Details see MPC8xx User's Manual.

4.2 Chip-Select-Definition

For TQM8xxL Chip-Select Lines are configured as follow:

	Memory	Startaddress (set-up with MON8xx Program)
CS0#	FLASH Bank 0,	0x40000000
CS1#	FLASH Bank 1 (when used)	(at the end of FLASH Bank 0)
CS2#	SDRAM	0x00000000
CS3#	CAN-Controller (when used)	(not configured)

4.3 Flash Memory

4.3.1 Flash Memory Organisation

1 or 2 memory banks
2 to 8 MByte
32-Bit memory
On-Board-programmable (Bootlader for Flash-Programming through the serial interface)
Standard: 4 MByte, 90 ns (4 Waitstates)

Access Time	Waitstates
75 ns	TBD
90 ns	4
120 ns	TBD
150 ns	TBD

Available Flash-EPROM's:

Used Chip	Capacity	Organisation per Chip	Bank 0	Bank 1
2x 29LV800-xxEC	2 MB	512 K x 16	2MB	
2x 29LV160-xxEC	4 MB	1 M x 16	4MB	
4x 29LV160-xxEC	8 MB	1 M x 16	4MB	4MB
Without internal FLASH	Only possible with external ROM / Flash !			

Separate Pin at the Module Connector for Programming Voltage (+ 12 V, only for Function "Set Sector Protection" / "Reset Sector Protection")

Hardware Write Protect, protected Sectors can not be changed without the extra Programming Voltage. (important for Bootsector) Not recommended due to AMD flash bug!

4.3.2 Flash Memory Configuration

The FLASH will be managed by the GPCM. Used Timing:

GPCM, ACS = 00, TRLX = 0, CSNT = 1, SCY = 4, EHTR = 1 (Normal Mode)

ACS = 11, TRLX = 1, CSNT = 1, SCY = 15, EHTR = 0 (Boot Mode)

The two 16-bit Flash of the 32-bit Bank have only one Write-Enable Signal. Therefore only 16- or 32-bit write mode is available. Single Byte can be programmed as follows:

1.Read out the word, which includes the Byte to change
2.Replace the Byte within the Word
3.Write the word back

The Address line A29 (bit 31 is the LSB of the Address lines !) is connected with the Address Line A0 of the Flash. Therefore, the Address bit has to be shifted to left by 2 bit.

Example: program 32-bit

	1st Buscycle		2nd Buscycle	
	Address	Data	Address	Data
Specification AMD	0x0555	0x00AA	0x02AA	0x0055
TQM8xxL	0x40001554	0x00AA00AA	0x40000AA8	0x00550055
	3rd Buscycle		4th Buscycle	
	Address	Data	Address	Data
Specification AMD	0x0555	0x00A0	PA	32 Bit Daten
TQM8xxL	0x40001554	0x00A000A0	PA	32 Bit Daten

PA: the address for programming is equal for both

4.4 SDRAM

4.4.1 SDRAM Organisation

synchronous dynamic RAM (SDRAM)
4 to 64 MByte (4, 16, 32, 64 MByte)
one Memory Bank with 32-Bit memory
external expandable with PS/2-Moduls (additionally external Busdriver necessary)
Standard: 16 MB, 100 Mhz, Access Time 3 + 2 (Single read)
2 + 1 + 1 + 1 + 2 (Burst read)
3 + 2 (Single write)
2 + 1 + 1 + 1 + 2 (Burst write)

Access Time:

Access Time	CLKOUT	Single Read	Burst Read	Single Write	Burst Write
>100 MHz	50 MHz	3 + 2	2 + 1 + 1 + 1 + 2	3 + 2	2 + 1 + 1 + 1 + 2

Available SDRAM on the Minimodule:

Used Chip	Capacity	Organisation per Chip	Bank 2
16 MBit	4 MB	1 M x 16	4 M
64 MBit	16 MB	4 M x 16	16 M
128 MBit	32 MB	8 M x 16	32 M
256 MBit	64 MB	16 M x 16	64 M
Without internal SDRAM	Only possible with external RAM!		

4.4.2 SDRAM Configuration

The SDRAM will be managed by the UPMA. The UPM is set-up for use SDRAM with single and burst read & write, CAS latency 2, sequential mode (no Interleave), 4 times Burst. The GPL will be used as:

CS2#	CS#
GPL_AB1	WE#
GPL_AB2	RAS#
GPL_AB3	CAS#
BS_AB[0:1]#	DQMU (MSB), DQML (upper word)
BS_AB[2:3]#	DQMU, DQML (LSB) (lower word)

The set-up for the Sequencer Table of the UPMA and other configurations to use a SDRAM are shown in the following .CMM-File. This can be used directly with the Lauterbach BDM-Debugger. For other Debugging Tools, it may be necessary to modify the syntax.

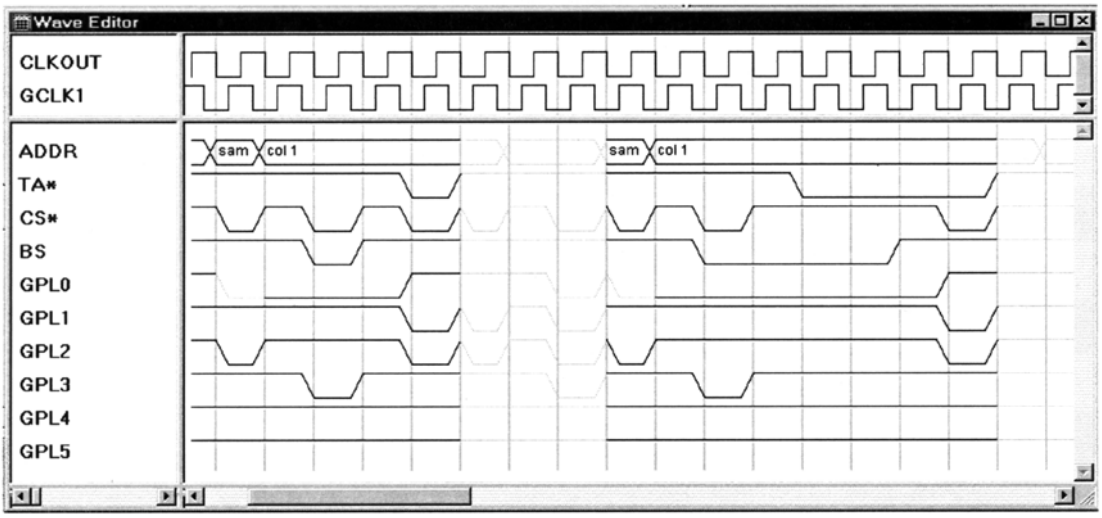
Remark: Both Monitor Program MON8xx and the following Script set the BI Bit within the Option Register of the SDRAM. This may cause problems, if you use the cache of the Microprocessor. In that case it is recommended to erase the BI-Bit. (Value for using Cache see comment in the script)

```
;  ===========================================================================
; Preliminary Memory Initialisation for TQM860
;  ===========================================================================
; ---------------------------------------------------------------------------
; System integration timers
; no need to change (1:1 clock mode)
; ---------------------------------------------------------------------------
; DATA.set 0FFF00284 %LONG 000000000

; ---------------------------------------------------------------------------
; Memory mapping
; ---------------------------------------------------------------------------
;           Initialisation BR0/1 and OR0/1 (FLASH)
DATA.set 0FFF00100 %LONG 040000001 /VERIFY
DATA.set 0FFF00104 %LONG 0E0000F52 /VERIFY
DATA.set 0FFF00108 %LONG 060000001 /VERIFY
DATA.set 0FFF0010C %LONG 0E0000F52 /VERIFY
                              ; from Rev. 200: 0E0000F50

;           Initialisation BR2/3 and OR2/3 (SDRAM)
DATA.set 0FFF00110 %LONG 000000081 /VERIFY
DATA.set 0FFF00114 %LONG 0E0000B00 /VERIFY ;(use with cache: 0E0000A00)
DATA.set 0FFF00118 %LONG 020000081 /VERIFY
DATA.set 0FFF0011C %LONG 0E0000B00 /VERIFY ;(use with cache: 0E0000A00)

;           Initialisation BR4 and OR4 (SRAM)
DATA.set 0FFF00120 %LONG 080000001 /VERIFY
DATA.set 0FFF00124 %LONG 0E0000D40 /VERIFY

; ---------------------------------------------------------------------------
; Programming UPMA (for SDRAM)
; ---------------------------------------------------------------------------
;           single read. (offset 0 in UPMA RAM)
DATA.set 0FFF0017C %LONG 01F0DFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002100 /VERIFY

DATA.set 0FFF0017C %LONG 0EEAFBC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002101 /VERIFY

DATA.set 0FFF0017C %LONG 011AF7C04 /VERIFY
DATA.set 0FFF00168 %LONG 000002102 /VERIFY

DATA.set 0FFF0017C %LONG 0EFBAFC00 /VERIFY
DATA.set 0FFF00168 %LONG 000002103 /VERIFY

DATA.set 0FFF0017C %LONG 01FF5FC47 /VERIFY
DATA.set 0FFF00168 %LONG 000002104 /VERIFY

;           SDRAM initialisation (offset 5)
DATA.set 0FFF0017C %LONG 01FF5FC34 /VERIFY
   DATA.set 0FFF00168 %LONG 000002105 /VERIFY

DATA.set 0FFF0017C %LONG 0EFEABC34 /VERIFY
DATA.set 0FFF00168 %LONG 000002106 /VERIFY
```

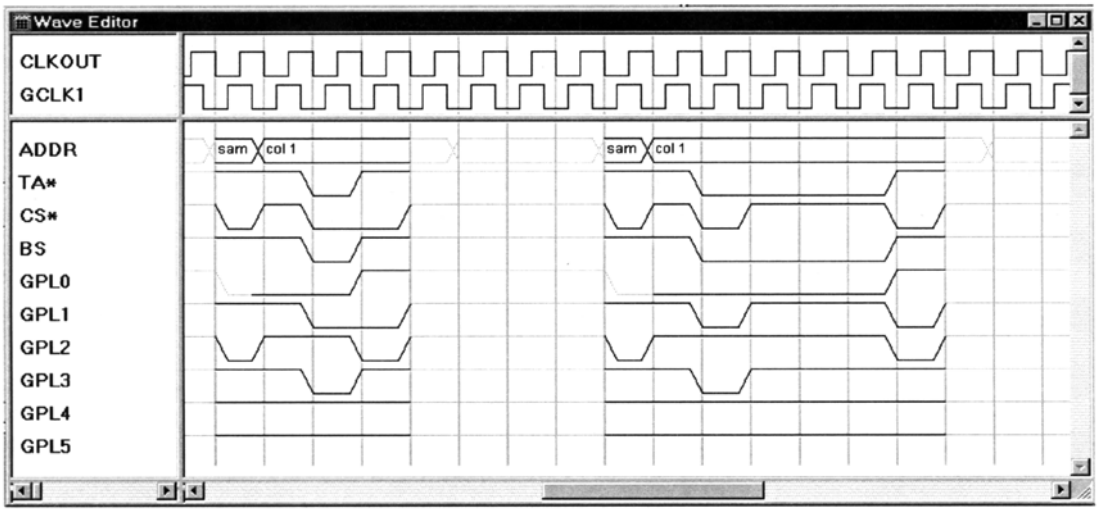
```
DATA.set 0FFF0017C %LONG 01FB57C35 /VERIFY
DATA.set 0FFF00168 %LONG 000002107 /VERIFY

;       burst read. (offset 8 in UPMA RAM)
DATA.set 0FFF0017C %LONG 01F0DFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002108 /VERIFY

DATA.set 0FFF0017C %LONG 0EEAFBC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002109 /VERIFY

DATA.set 0FFF0017C %LONG 010AF7C04 /VERIFY
DATA.set 0FFF00168 %LONG 00000210A /VERIFY

DATA.set 0FFF0017C %LONG 0F0AFFC00 /VERIFY
DATA.set 0FFF00168 %LONG 00000210B /VERIFY

DATA.set 0FFF0017C %LONG 0F0AFFC00 /VERIFY
DATA.set 0FFF00168 %LONG 00000210C /VERIFY

DATA.set 0FFF0017C %LONG 0F1AFFC00 /VERIFY
DATA.set 0FFF00168 %LONG 00000210D /VERIFY

DATA.set 0FFF0017C %LONG 0EFBAFC00 /VERIFY
DATA.set 0FFF00168 %LONG 00000210E /VERIFY

DATA.set 0FFF0017C %LONG 01FF5FC47 /VERIFY
DATA.set 0FFF00168 %LONG 00000210F /VERIFY

;       single write. (offset 18 in UPMA RAM)
DATA.set 0FFF0017C %LONG 01F2DFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002118 /VERIFY

DATA.set 0FFF0017C %LONG 0EEABBC00 /VERIFY
DATA.set 0FFF00168 %LONG 000002119 /VERIFY

DATA.set 0FFF0017C %LONG 001B27C04 /VERIFY
DATA.set 0FFF00168 %LONG 00000211A /VERIFY

DATA.set 0FFF0017C %LONG 01FF5FC47 /VERIFY
DATA.set 0FFF00168 %LONG 00000211B /VERIFY

;       burst write. (offset 20 in UPMA RAM)
DATA.set 0FFF0017C %LONG 01F0DFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002120 /VERIFY

DATA.set 0FFF0017C %LONG 0EEABBC00 /VERIFY
DATA.set 0FFF00168 %LONG 000002121 /VERIFY

DATA.set 0FFF0017C %LONG 010A77C00 /VERIFY
DATA.set 0FFF00168 %LONG 000002122 /VERIFY

DATA.set 0FFF0017C %LONG 0F0AFFC00 /VERIFY
DATA.set 0FFF00168 %LONG 000002123 /VERIFY

DATA.set 0FFF0017C %LONG 0F0AFFC00 /VERIFY
DATA.set 0FFF00168 %LONG 000002124 /VERIFY

DATA.set 0FFF0017C %LONG 0E1BAFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002125 /VERIFY

DATA.set 0FFF0017C %LONG 01FF5FC47 /VERIFY
DATA.set 0FFF00168 %LONG 000002126 /VERIFY

;       refresh  (offset 30 in UPMA RAM)
```

```
DATA.set 0FFF0017C %LONG 01FFD7C84 /VERIFY
DATA.set 0FFF00168 %LONG 000002130 /VERIFY

DATA.set 0FFF0017C %LONG 0FFFFFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002131 /VERIFY

DATA.set 0FFF0017C %LONG 0FFFFFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002132 /VERIFY

DATA.set 0FFF0017C %LONG 0FFFFFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002133 /VERIFY

DATA.set 0FFF0017C %LONG 0FFFFFC84 /VERIFY
DATA.set 0FFF00168 %LONG 000002134 /VERIFY

DATA.set 0FFF0017C %LONG 0FFFFFC07 /VERIFY
DATA.set 0FFF00168 %LONG 000002135 /VERIFY

;       exception. (offset 3c in UPMA RAM)
DATA.set 0FFF0017C %LONG 07FFFFC07 /VERIFY
DATA.set 0FFF00168 %LONG 00000213C /VERIFY

; ---------------------------------------------------------------------------
; Refresh and Initialisation for SDRAM
; ---------------------------------------------------------------------------
;       initialise machine mode a Register (MAMR)
DATA.set 0FFF00170 %LONG 0C3802114 /VERIFY

;       initialise memory periodic timer prescaler (MPTPR)
;       Preliminary prescaler for refresh (depends on number of banks). This value
;       is selected for four cycles every 62.4 us with two SDRAM banks or four
;       cycles every 31.2 us with one bank. It will be adjusted after memory sizing.
DATA.set 0FFF0017A %WORD 01000 /VERIFY

;       initialise memory address register (MAR)
DATA.set 0FFF00164 %LONG 000000088 /VERIFY

;       precharge-all start Commando via Memory Command Register at Patch-Offset $5
;       The SDRAM-Initialisation starts from Patch-Offset $7!!
;       Baenke 0 und 1
DATA.set 0FFF00168 %LONG 080004105 /VERIFY
DATA.set 0FFF00168 %LONG 080006105 /VERIFY

;       2 x 4 times-Refresh starts via Memory Command Register at the Patch-Offset $30
DATA.set 0FFF00168 %LONG 080004130 /VERIFY
DATA.set 0FFF00168 %LONG 080004130 /VERIFY
DATA.set 0FFF00168 %LONG 080006130 /VERIFY
DATA.set 0FFF00168 %LONG 080006130 /VERIFY
```

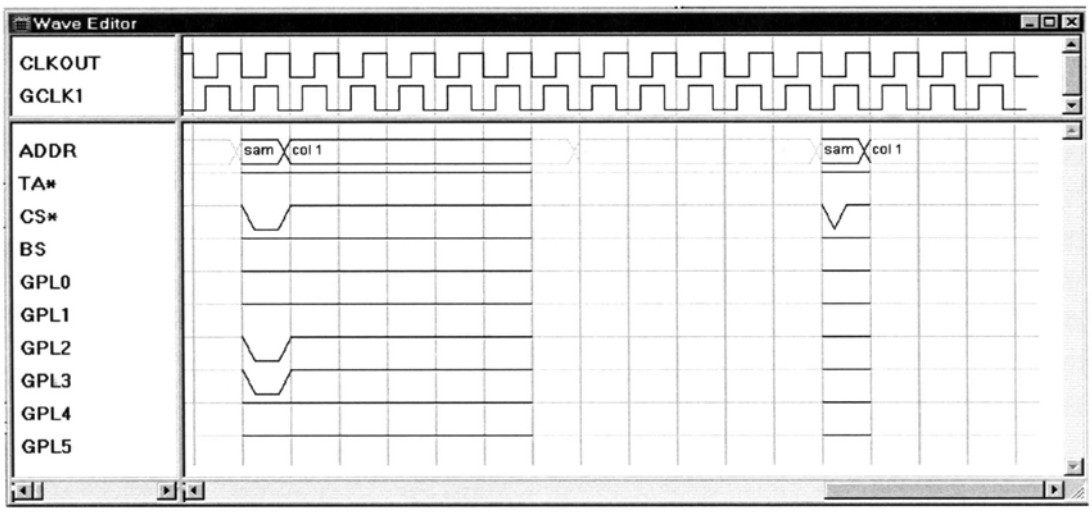
This results in the following Access Signals:
Single read and Burst read



Single write and Burst write



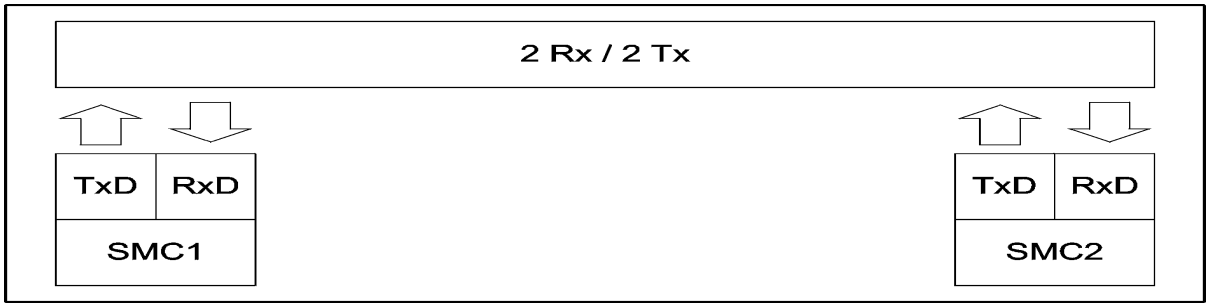
Refresh and Exception



5 Interface

5.1 Serial Interface

max. 115200 Baud
Short-Circuit protected RS232-Driver for 2 UARTs
all Signals also available without drivers
Standard: Driver for 2x RxD/TxD



5.2 TQ-Download-Interface

RxD and TxD
Reset via RS232-Interface
Additional input line from RS232 Interface (read out through Port-Pin)
All signals on the Minimodule Board to Board Connector

For first set-up of the Minimodule, it is recommended to use the EVA-Board for TQM8xxL Minimodule with Power Supply and TQC-Download Interface (through serial Interface)

The debugging Interface has the following Signals:

Pin	Signalname	Typ	Function
X1-41	ENMON#/BOOT	I	Switch from Monitor mode to normal Boot Mode
X1-51	TXD2	O	TxD of Debugging-Interface (SCC2, RS232-Signal level)
X1-01	GND	-	Digital Ground
X1-34	RESIN#	I	Reset-Input (Master-Reset of Reset-Chip)
X1-50	RXD2	I	RxD of Debugging-Interface (SCC2, RS232-Signal level)

5.3 EBDI/BDM-Interface

All Lines of Motorola EBDI (Enhanced Background Debugging Interface)
direct access on all registers and memories (need extra Hardware EBDI or EBDI-Lite and EBDS Software)
Same as the TQC Debugging Interface the BDM / EBDI Interface will be available at the Minimodule Board to Board Connector. He BDM / EBDI Interface has following Signals:

Pin	Signalname	Typ	Function
	VFSL0	O	CPU history buffer status
X1-42	SRESET#	I/O	Soft reset
X1-01	DGND	-	Masse
X2-46	TCK/DSCK	I	Clock
	VFLS1	O	CPU history buffer status
X1-37	HRESET#	I/O	Hard reset
X2-44	TDI/DSDI	I	Data input
X2-45	TDO/DSDO	O	Data output

Instead of VFSL0,1 Pins, FRZ# Pin can be used.

5.4 Bus interface for external access

26 / 32 Bit Address- and 32 Bit Data-Bus
8-, 16- and 32-Bit-Access
Timing programmable
DMA or CPU-Access
All I/O- and Control-Lines available

Details see MPC8xx User's Manual.

5.5 CAN Interface

5.5.1 General CAN Interface

2 CAN Controllers Intel 82527
Using Interrupt Request 4 (IRQ4#)
CAN is addressed via CS3#, A22 and A23

	CAN 1	CAN 2
CS3#	0	0
A22	0	0
A23	0	1

5.5.2 CAN Interface Configuration

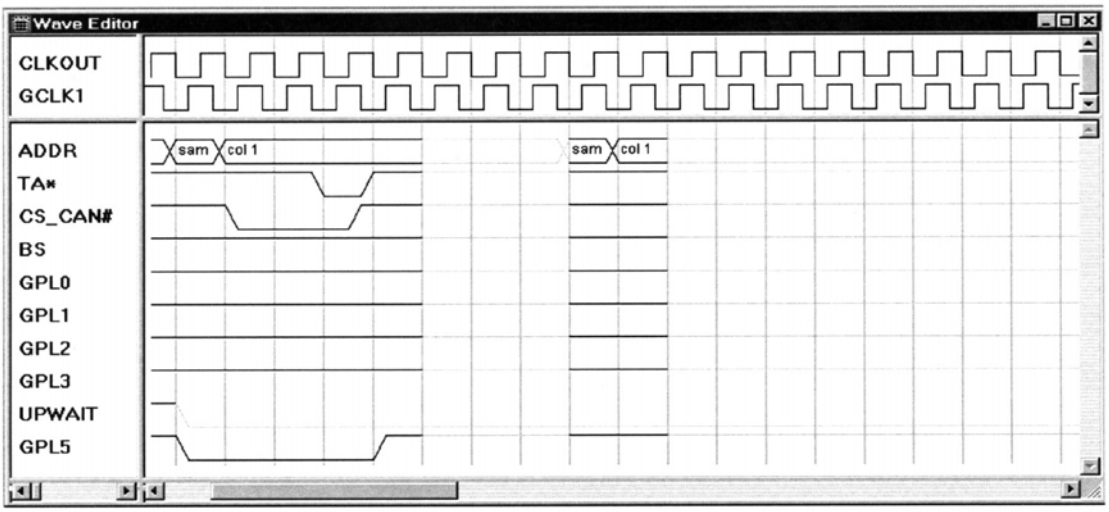
The Access Time for the CAN Controller 82527 varies depending on actual and last Access. To optimise the access to the CAN Controller the Acknowledge Signal of the 82527 Chip will be used. In that case a UPM is necessary. The UPMB is used and the following Signals are generated:

CS3#, A22, A23	CS# (via Multiplexer) see 5.5.1
GPL_AB2#	R / W#
UPWAITB / GPL_B4#	DSACK0#
GPL_A5#	Buffer Enable for Data Bus AD[15:8]

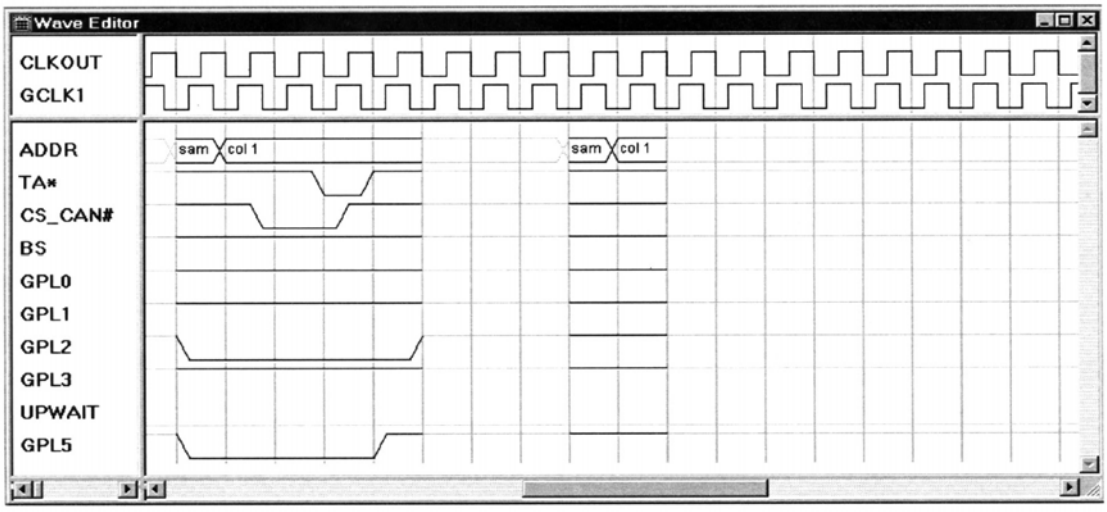
In the following Example both CAN Controller will be mapped to Address 0xC0000000. The set-up for the Sequencer Table of the UPMA and other configurations to use a CAN Interface are shown in the following .CMM-File. This can be used directly with the Lauterbach BDM-Debugger. For other Debugging Tools it may be necessary to modify the syntax.

```
;  ===========================================================================
; Preliminary CAN Access for TQM8xxL
;  ===========================================================================


; CAN-Access @ 50 MHz, R/W#-CAN and BUFOE# through GPLs

;                               Initialisation BR2 and OR2 (CAN 1-2)
DATA.SET 0FFF00118 %LONG 0C00004C1 /VERIFY
DATA.SET 0FFF0011C %LONG 0FFFF8500 /VERIFY

;                               Initialisation MBMR to manage both CAN-Controller
DATA.SET 0FFF00174 %LONG 00001000 /VERIFY
;DATA.SET 0FFF00174 %LONG 00000000 /VERIFY

; SIUMCR GPL5 activating
; DATA.SET 0FFF00000 %long 001600040 /verify

; Initialisation of Micropatches for UPMB/CAN
; single read
DATA.SET 0FFF0017C %LONG 0ffffc004 /VERIFY
DATA.SET 0FFF00168 %LONG 000800100 /VERIFY

DATA.SET 0FFF0017C %LONG 00fffd004 /VERIFY
DATA.SET 0FFF00168 %LONG 000800101 /VERIFY

DATA.SET 0FFF0017C %LONG 00fffc000 /VERIFY
DATA.SET 0FFF00168 %LONG 000800102 /VERIFY

DATA.SET 0FFF0017C %LONG 03fffc004 /VERIFY
DATA.SET 0FFF00168 %LONG 000800103 /VERIFY

DATA.SET 0FFF0017C %LONG 0ffffdc05 /VERIFY
DATA.SET 0FFF00168 %LONG 000800104 /VERIFY

; single write
DATA.SET 0FFF0017C %LONG 0fffcc004 /VERIFY
DATA.SET 0FFF00168 %LONG 000800118 /VERIFY

DATA.SET 0FFF0017C %LONG 0cffcd004 /VERIFY
DATA.SET 0FFF00168 %LONG 000800119 /VERIFY

DATA.SET 0FFF0017C %LONG 00ffcc000 /VERIFY
DATA.SET 0FFF00168 %LONG 00080011A /VERIFY

DATA.SET 0FFF0017C %LONG 07ffcc004 /VERIFY
DATA.SET 0FFF00168 %LONG 00080011B /VERIFY

DATA.SET 0FFF0017C %LONG 0fffdcc05 /VERIFY
DATA.SET 0FFF00168 %LONG 00080011C /VERIFY

; disable global Chip Select (CS0#)
DATA.SET 0FFF00100 %LONG 000000000 /VERIFY

; Configuration 82527
; MCLK 8 MHz (@fXTAL = 16 MHz), ISO low speed phys. layer active
; (-> P2.6 = INT#), CLKOUT active (both CAN-Controller)
DATA.SET 0C0000002 %byte 045 /VERIFY
DATA.SET 0C0000102 %byte 045 /VERIFY
```

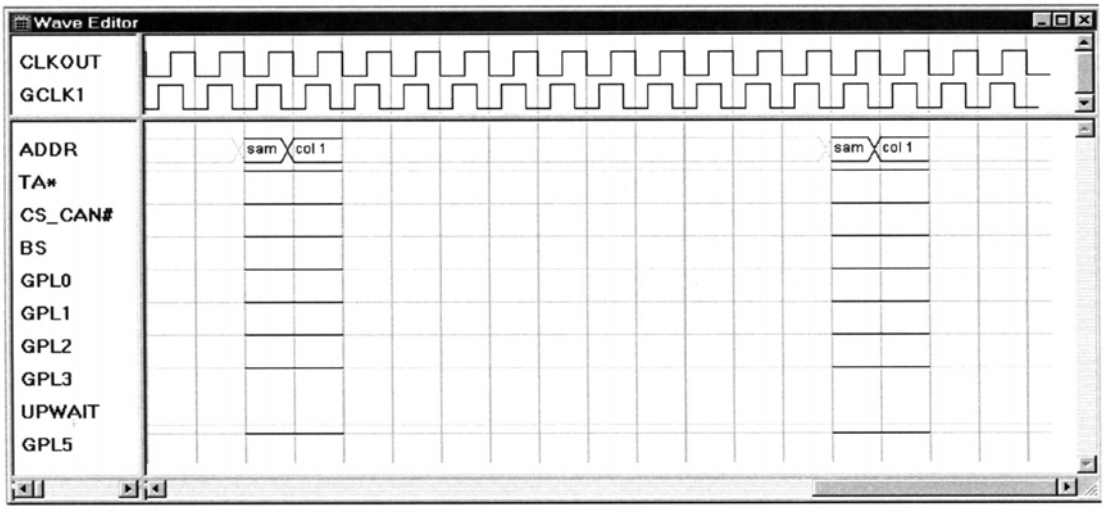
This results in the following Access Signals:
Single read and Burst read



Single write and Burst write



Refresh and Exception



5.6 Module Signal Description

This chapter describes the function of the TQM850L and TQM823L connections.

5.6.1 CPU Pins for TQM823L and TQM850L

Signal	CPU-Pin	Module-Pin	Type	Description TQM823L / TQM850L
D0	M1	X2-88	I/O, TS	Data Bus D0 (MSB)
D1	L1	X2-89	I/O, TS	Data Bus D1
D2	l2	X2-90	I/O, TS	Data Bus D2
D3	l1	X2-91	I/O, TS	Data Bus D3
D4	L2	X2-92	I/O, TS	Data Bus D4
D5	H1	X2-93	I/O, TS	Data Bus D5
D6	F1	X2-94	I/O, TS	Data Bus D6
D7	E1	X2-95	I/O, TS	Data Bus D7
D8	M2	X2-96	I/O, TS	Data Bus D8
D9	K2	X2-97	I/O, TS	Data Bus D9
D10	K3	X2-98	I/O, TS	Data Bus D10
D11	K1	X2-99	I/O, TS	Data Bus D11
D12	M4	X2-100	I/O, TS	Data Bus D12
D13	M3	X2-101	I/O, TS	Data Bus D13
D14	l3	X2-102	I/O, TS	Data Bus D14
D15	l4	X2-103	I/O, TS	Data Bus D15
D16	H2	X2-104	I/O, TS	Data Bus D16
D17	K4	X2-105	I/O, TS	Data Bus D17
D18	H3	X2-106	I/O, TS	Data Bus D18
D19	G2	X2-107	I/O, TS	Data Bus D19
D20	G3	X2-108	I/O, TS	Data Bus D20
D21	F2	X2-109	I/O, TS	Data Bus D21
D22	H4	X2-110	I/O, TS	Data Bus D22
D23	L4	X2-111	I/O, TS	Data Bus D23
D24	F3	X2-112	I/O, TS	Data Bus D24
D25	G4	X2-113	I/O, TS	Data Bus D25
D26	E4	X2-114	I/O, TS	Data Bus D26
D27	L3	X2-115	I/O, TS	Data Bus D27
D28	F4	X2-116	I/O, TS	Data Bus D28
D29	E2	X2-117	I/O, TS	Data Bus D29
D30	D2	X2-118	I/O, TS	Data Bus D30
D31	E3	X2-119	I/O, TS	Data Bus D31 (LSB)
RES/A0	-	X1-111	-	Reserved
RES/A1	-	X1-110	-	Reserved
RES/A2	-	X1-109	-	Reserved
RES/A3	-	X1-108	-	Reserved
RES/A4	-	X1-107	-	Reserved
RES/A5	-	X1-106	-	Reserved
A6	M13	X1-105	I/O, TS	Address Bus A6
A7	N15	X1-104	I/O, TS	Address Bus A7
A8	N16	X1-103	I/O, TS	Address Bus A8
A9	M15	X1-102	I/O, TS	Address Bus A9
A10	L13	X1-101	I/O, TS	Address Bus A10
A11	M16	X1-100	I/O, TS	Address Bus A11
A12	M14	X1-99	I/O, TS	Address Bus A12
A13	L14	X1-98	I/O, TS	Address Bus A13
A14	L15	X1-97	I/O, TS	Address Bus A14
A15	L16	X1-96	I/O, TS	Address Bus A15
A16	K14	X1-95	I/O, TS	Address Bus A16

Signal	CPU-Pin	Module-Pin	Type	Description TQM823L / TQM850L
A17	K13	X1-94	I/O, TS	Address Bus A17
A18	G13	X1-93	I/O, TS	Address Bus A18
A19	K15	X1-92	I/O, TS	Address Bus A19
A20	I15	X1-91	I/O, TS	Address Bus A20
A21	I14	X1-90	I/O, TS	Address Bus A21
A22	G14	X1-89	I/O, TS	Address Bus A22
A23	H15	X1-88	I/O, TS	Address Bus A23
A24	H13	X1-87	I/O, TS	Address Bus A24
A25	H14	X1-86	I/O, TS	Address Bus A25
A26	F14	X1-85	I/O, TS	Address Bus A26
A27	K16	X1-84	I/O, TS	Address Bus A27
A28	G16	X1-83	I/O, TS	Address Bus A28
A29	H16	X1-82	I/O, TS	Address Bus A29
A30	G15	X1-81	I/O, TS	Address Bus A30
A31	F16	X1-80	I/O, TS	Address Bus A31 (LSB)
RES / PA0	-	X2-28	-	Reserved
RES / PA1	-	X2-29	-	Reserved
RES / PA2	-	X2-30	-	Reserved
RES / PA3	-	X2-31	-	Reserved
PA4	R6	X2-32	I/O	Port PA4 - direct connected
PA5	T6	X2-33	I/O	Port PA5 - direct connected
PA6	P8	X2-34	I/O	Port PA6 - direct connected
PA7	T8	X2-35	I/O	Port PA7 - direct connected
SMTXD2# PA8	T9	X2-36	I/O	Port PA8 used as SMTXD2#, connected to RS232-Driver TTL-Input (Driver Output X1-51)
SMRXD2# PA9	N10	X2-37	I/O	Port PA9 used as SMRXD2#, connected to RS232-Driver TTL-Output via a 4k7 resistor for decoupling for other usage (Driver Input X1-50)
RES / PA10	-	X2-38	-	Reserved
RES / PA11	-	X2-39	-	Reserved
PA12	R13	X2-40	I/O	Port PA12 - direct connected
PA13	R14	X2-41	I/O	Port PA13 - direct connected
PA14	R15	X2-42	I/O	Port PA14 - direct connected
PA15	P16	X2-43	I/O	Port PA15 - direct connected
RES / PB14	-	X2-48	-	Reserved
RES / PB15	-	X2-49	-	Reserved
PB16	R5	X2-50	I/O	Port PB16 - direct connected
PB17	N7	X2-51	I/O	Port PB17 - direct connected
PB18	P7	X2-52	I/O	Port PB18 - direct connected
PB19	R7	X2-53	I/O	Port PB19 - direct connected
RES / PB20	-	X2-54	-	Reserved
RES / PB21	-	X2-55	-	Reserved
PB22	R9	X2-56	I/O	Port PB22 - direct connected
PB23	T10	X2-57	I/O	Port PB23 - direct connected
SMRXD1# RXD3# PB24	T11	X2-58	I/O	Port PB24 used as SMRXD1# or RXD3#, connected to RS232-Driver TTL-Output via a 4k7 resistor for decoupling for other usage (Driver Input X1-52)

Signal	CPU-Pin	Module-Pin	Type	Description TQM823L / TQM850L
SMTXD1# TXD3# PB25	N11	X2-59	I/O	Port PB25 used as SMTXD1# or TXD3#, connected to RS232-Driver TTL-Input (Driver Output X1-53)
PB26	P12	X2-60	I/O	Port PB26 - direct connected
PB27	T14	X2-61	I/O	Port PB27 - direct connected
PB28	T15	X2-62	I/O	Port PB28 - direct connected
PB29	P14	X2-63	I/O	Port PB29 - direct connected
PB30	P15	X2-64	I/O	Port PB30 - direct connected
PB31	N14	X2-65	I/O	Port PB31 - direct connected
PC4	T4	X2-16	I/O	Port PC4 - direct connected
PC5	P6	X2-17	I/O	Port PC5 - direct connected
PC6	N6	X2-18	I/O	Port PC6 - direct connected
PC7	T5	X2-19	I/O	Port PC7 - direct connected
PC8	N8	X2-20	I/O	Port PC8 - direct connected
PC9	R8	X2-21	I/O	Port PC9 - direct connected
PC10	P9	X2-22	I/O	Port PC10 - direct connected
PC11	R10	X2-23	I/O	Port PC11 - direct connected
PC12	T13	X2-24	I/O	Port PC12 - direct connected
PC13	P13	X2-25	I/O	Port PC13 - direct connected
PC14	T16	X2-26	I/O	Port PC14 - direct connected
PC15	R16	X2-27	I/O	Port PC15 - direct connected
PD3	N4	X2-3	I/O	Port PD3 - direct connected
PD4	P3	X2-4	I/O	Port PD4 - direct connected
PD5	P2	X2-5	I/O	Port PD5 - direct connected
PD6	R1	X2-6	I/O	Port PD6 - direct connected
PD7	R2	X2-7	I/O	Port PD7 - direct connected
PD8	T1	X2-8	I/O	Port PD8 - direct connected
PD9	P4	X2-9	I/O	Port PD9 - direct connected
PD10	T2	X2-10	I/O	Port PD10 - direct connected
PD11	N5	X2-11	I/O	Port PD11 - direct connected
PD12	R3	X2-12	I/O	Port PD12 - direct connected
PD13	P5	X2-13	I/O	Port PD13 - direct connected
PD14	T3	X2-14	I/O	Port PD14 - direct connected
PD15	R4	X2-15	I/O	Port PD15 - direct connected
IRQ0#	N1	X1-2	I	Interrupt Request 0, pull-up 4k7
IRQ1#	N2	X1-3	I	Interrupt Request 1, pull-up 4k7
IRQ2# RSV#	D9	X1-4	I/O, TS	Interrupt Request 2 / Reservation, pull-up 4k7
IRQ3#	C3	X1-5	I/O, TS	Interrupt Request 3, pull-up 4k7
IRQ_CAN# IRQ4#	D4	X1-6	I/O, TS	Interrupt Request 4 used as CAN Interrupt, connected to P2.6/INT# of both AS82527 devices, pull-up 4k7
IRQ5#	D3	X1-7	I/O, TS	Interrupt Request 5, pull-up 4k7
IRQ6#	C2	X1-8	I/O, TS	Interrupt Request 6, pull-up 4k7
IRQ7#	N3	X1-9	I	Interrupt Request 7, pull-up 4k7
CLKOUT	D1	X1-40	O	System Clock Output
EXTCLK	A6	X1-39	I/O	External Clock Input - only for special Versions
TEXP	D5	X1-36	O	Timer Expired Output - direct connected

Signal	CPU-Pin	Module-Pin	Type	Description TQM823L / TQM850L
PORESET#	B3	X1-35	O	Power-On Reset connected to Reset Device / Voltage Supervisor for 3,3 and 5 V
HRESET#	B5	X1-37	I/O, OD	Hard Reset, pull-up 1k
SRESET#	B4	X1-42	I/O, OD	Soft Reset, pull-up 10k, Switch Reset-LED
RSTCONF#	C5	X1-38	I	Reset Configuration, Pull-Down 1k
DSDI/TDI	R11	X2-44	I	Development Serial Data Input / Test Data Input, Pull-down 10k
DSDO/TDO	N12	X2-45	O, TS	Development Serial Data Output / Test Data Output - direct connected
DSCK/TCK	T12	X2-46	I	Development Serial Clock / Test Clock, Pull-Down 1k
TMS	R12	X2-47	I	Test Mode Select, pull-up 10k
RES / BS_A0#	-	X1-56	-	Reserved
RES / BS_A1#	-	X1-57	-	Reserved
RES / BS_A2#	-	X1-58	-	Reserved
RES / BS_A3#	-	X1-59	-	Reserved
WE0# BS_AB0#	D16	X1-76	O	Write Enable / Byte Select 0
WE1# BS_AB1#	E16	X1-77	O	Write Enable / Byte Select 1
WE2# BS_AB2#	D15	X1-78	O	Write Enable / Byte Select 2
WE3# BS_AB3#	F13	X1-79	O	Write Enable / Byte Select 3
CS_FLASH0# CS0#	D12	X1-71	O	Chip Select 0 used as (Boot) FLASH Chip Select
CS_FLASH1# CS1#	A14	X1-70	O	Chip Select 1 used as FLASH Chip Select
CS_SDRAM0-# CS2#	B14	X1-69	O	Chip Select 2 used as SDRAM Chip Select
CS_CAN# CS3#	A15	X1-68	O	Chip Select 3 used as CAN Chip Select
CS4#	B16	X1-67	O	Chip Select 4 - direct connected
CS5#	D13	X1-66	O	Chip Select 5 - direct connected
CS6# CE_1B#	C14	X1-65	O	Chip Select 6 / Card Enable 1 Slot B - direct connected
CS7# CE_2B#	B15	X1-64	O	Chip Select 7 / Card Enable 2 Slot B - direct connected
RES / CE1_A#	-	X1-54	-	Reserved
RES / CE2_A#	-	X1-55	-	Reserved
RD / WR#	C13	X2-73	O	Read / Write RD/WR#
BB#	A11	X2-75	I/O	Bus Busy, pull-up 2k2
BG#	C10	X2-74	I/O	Bus Grant - direct connected
BR#	B11	X2-76	I/O	Bus Request, pull-up 4k7
BURST#	B10	X2-82	I/O, TS	Burst Transaction - direct connected
B#	B12	X2-81	I/O, TS	Burst Inhibit, pull-up 4k7
BDIP# GPL_B5#	A13	X1-63	I/O, TS	Burst Data in Progress General Purpose Line B5 - direct connected
GPL_A5#	C12	X1-62	O	General Purpose Line A5 used for CAN
UPWAITB	B13	X1-61	I/O	User Programmable Machine Wait B
GPL_B4#				General Purpose Line B4 - direct connected

Signal	CPU-Pin	Module-Pin	Type	Description TQM823L / TQM850L
UPWAITA GPL_A4	D11	X1-60	I/O	User Programmable Machine Wait A General Purpose Line A4 used for CAN
GPL_AB3#	D14	X1-75	O	General Purpose Line A3 / B3 used for SDRAM
GPL_AB2#	C15	X1-74	O	General Purpose Line A2 / B2 used for SDRAM and CAN
OE# GPL_AB1#	C16	X1-73	O	Output Enable General Purpose Line A1 / B1 used for SDRAM and FLASH
GPL_AB0#	E13	X1-72	O	General Purpose Line A0 / B0 - direct connected
RES / WAIT_A#	-	X1-10	-	Reserved
RES / ALE_A	-	X1-11	-	Reserved
RES / IPA0	-	X1-12	-	Reserved
RES / IPA1	-	X1-13	-	Reserved
RES / IPA2	-	X1-14	-	Reserved
RES / IPA3	-	X1-15	-	Reserved
RES / IPA4	-	X1-16	-	Reserved
RES / IPA5	-	X1-17	-	Reserved
RES / IPA6	-	X1-18	-	Reserved
RES / IPA7	-	X1-19	-	Reserved
WAIT_B#	C4	X1-24	I	Wait Slot B, pull-up 4k7
ALE_B	B8	X1-25	I/O, TS	Address Latch Enable Slot B, pull-up 4k7
IPB0	A8	X1-33	I	Input Port B0, pull-up 4k7
IPB1	C8	X1-32	I	Input Port B1, pull-up 4k7
IPB2	D7	X1-31	I	Input Port B2, pull-up 4k7
IPB3	A9	X1-30	I	Input Port B3, pull-up 4k7
IPB4	B9	X1-29	I	Input Port B4, pull-up 4k7
IPB5	C9	X1-28	I	Input Port B5, pull-up 4k7
IPB6	C7	X1-27	I	Input Port B6, pull-up 4k7
IPB7	D8	X1-26	I	Input Port B7, pull-up 4k7
RES / OP0	-	X1-21	-	Reserved
RES / OP1	-	X1-20	-	Reserved
MODCK1 OP2	D6	X1-22	I/O	Mode Clock 1 Output Port 2
MODCK2 OP3	B6	X1-23	I/O	Mode Clock 2 Output Port 3
TS#	D10	X2-83	I/O, TS	Transfer Start, pull-up 4k7
TA#	A12	X2-77	I/O, TS	Transfer Acknowledge, pull-up 2k2
TEA#	C11	X2-80	I/O, OD	Transfer Error Acknowledge, pull-up 2k2
TSIZ0 REG#	F15	X2-78	I/O, TS	Transfer Size 0 / Register - direct connected
TSIZ1	E15	X2-79	I/O, TS	Transfer Size 1 - direct connected
IRQ4# KR# RETRY	B7	X2-72	I/O	Interrupt Request 4 / Kill Reservation / Retry, pull-up 4k7
RES / CR#	-	X2-70	-	Reserved
FRZ / IRQ6#	A10	X2-71	I/O	Freeze / Interrupt Request 6, pull-up 4k7
RES / AS#	-	X2-69	-	Reserved
RES / BADDR28	-	X2-68	-	Reserved
RES / BADDR29	-	X2-67	-	Reserved
RES / BADDR30	-	X2-66	-	Reserved
Spare1	-	X2-87	-	Reserved
Spare2	P10	X2-86	-	Spare2
Spare3	P1	X2-85	-	Spare3
Spare4	-	X2-84	-	Reserved

5.6.2 Non-CPU Pins for TQM823L and TQM850L

Signal	Type	Module-Pin	Description TQM823L / TQM850L
VCC3V3	-	X1-112 X1-113 X1-114	3.3 V Supply
VCC5V	-	X1-116 X1-118 X1-120	5 V Supply
VBAT	-	X2-1	Battery Input, connected to KAPWR via Schottky Diode
DGND	-	X1-1 X1-115 X1-117 X1-119 X2-2 X2-120	Digital Ground
SMRXD1	I	X1-52	SMRXD1# via RS232 receiver
SMTXD1	O	X1-53	SMTXD1# via RS232 driver
SMRXD2	I	X1-50	SMRXD2# via RS232 receiver
SMTXD2	O	X1-51	SMTXD2# via RS232 driver
RX0-CAN1	I	X1-49	Single-Ended CAN Receive 1
TX0-CAN1	O	X1-48	Single-Ended CAN Transmit 1
RX0-CAN2	I	X1-47	Single-Ended CAN Receive 2
TX0-CAN2	O	X1-46	Single-Ended CAN Transmit 2
ENMON#	I	X1-41	Enable Monitor. Pull low to enable MON8xx after Reset. Must be stable for min. 50 ms after PORESET becomes inactive. pull-up 10k.
JTAG BDM#	I	X1-43	JTAG / BDM Select. Pull low to enable BDM. pull-up 10k.
HRESETF#	I	X1-44	Hard Reset at FLASH. Can be used to connect 12 V to FLASHes' RESET pin without damage to the module.
CKE	I	X1-45	Clock Enable of SDRAMs. May be pulled low to enter SDRAM Power Down. pull-up 4k7.
RESIN#	I	X1-34	Reset Input. Connected to Reset device. pull-up 4k7.

5.6.3 CPU Pins for TQM855L / TQM860L

This chapter describes the function of theTQM855L / TQM860L connections.

Signal	CPU-Pin	Module-Pin	Type	Description TQM855L / TQM860L
D0	W14	X2-88	I/O, TS	Data Bus D0 (MSB)
D1	W12	X2-89	I/O, TS	Data Bus D1
D2	W11	X2-90	I/O, TS	Data Bus D2
D3	W10	X2-91	I/O, TS	Data Bus D3
D4	W13	X2-92	I/O, TS	Data Bus D4
D5	W9	X2-93	I/O, TS	Data Bus D5
D6	W7	X2-94	I/O, TS	Data Bus D6
D7	W6	X2-95	I/O, TS	Data Bus D7
D8	U13	X2-96	I/O, TS	Data Bus D8
D9	T11	X2-97	I/O, TS	Data Bus D9
D10	V11	X2-98	I/O, TS	Data Bus D10
D11	U11	X2-99	I/O, TS	Data Bus D11
D12	T13	X2-100	I/O, TS	Data Bus D12
D13	V13	X2-101	I/O, TS	Data Bus D13
D14	V10	X2-102	I/O, TS	Data Bus D14
D15	T10	X2-103	I/O, TS	Data Bus D15
D16	U10	X2-104	I/O, TS	Data Bus D16
D17	T12	X2-105	I/O, TS	Data Bus D17
D18	V9	X2-106	I/O, TS	Data Bus D18
D19	U9	X2-107	I/O, TS	Data Bus D19
D20	V8	X2-108	I/O, TS	Data Bus D20
D21	U8	X2-109	I/O, TS	Data Bus D21
D22	T9	X2-110	I/O, TS	Data Bus D22
D23	U12	X2-111	I/O, TS	Data Bus D23
D24	V7	X2-112	I/O, TS	Data Bus D24
D25	T8	X2-113	I/O, TS	Data Bus D25
D26	U7	X2-114	I/O, TS	Data Bus D26
D27	V12	X2-115	I/O, TS	Data Bus D27
D28	V6	X2-116	I/O, TS	Data Bus D28
D29	W5	X2-117	I/O, TS	Data Bus D29
D30	U6	X2-118	I/O, TS	Data Bus D30
D31	T7	X2-119	I/O, TS	Data Bus D31 (LSB)
A0	B19	X1-111	I/O, TS	Address Bus A0 (MSB)
A1	B18	X1-110	I/O, TS	Address Bus A1
A2	A18	X1-109	I/O, TS	Address Bus A2
A3	C16	X1-108	I/O, TS	Address Bus A3
A4	B17	X1-107	I/O, TS	Address Bus A4
A5	A17	X1-106	I/O, TS	Address Bus A5
A6	B16	X1-105	I/O, TS	Address Bus A6
A7	A16	X1-104	I/O, TS	Address Bus A7
A8	D15	X1-103	I/O, TS	Address Bus A8
A9	C15	X1-102	I/O, TS	Address Bus A9
A10	B15	X1-101	I/O, TS	Address Bus A10
A11	A15	X1-100	I/O, TS	Address Bus A11
A12	C14	X1-99	I/O, TS	Address Bus A12
A13	B14	X1-98	I/O, TS	Address Bus A13
A14	A14	X1-97	I/O, TS	Address Bus A14
A15	D12	X1-96	I/O, TS	Address Bus A15
A16	C13	X1-95	I/O, TS	Address Bus A16
A17	B13	X1-94	I/O, TS	Address Bus A17
A18	D9	X1-93	I/O, TS	Address Bus A18
A19	D11	X1-92	I/O, TS	Address Bus A19

Signal	CPU-Pin	Module-Pin	Type	Description TQM855L / TQM860L
A20	**C12**	**X1-91**	**I/O, TS**	**Address Bus A20**
A21	**B12**	**X1-90**	**I/O, TS**	**Address Bus A21**
A22	**B10**	**X1-89**	**I/O, TS**	**Address Bus A22**
A23	**B11**	**X1-88**	**I/O, TS**	**Address Bus A23**
A24	C11	X1-87	I/O, TS	Address Bus A24
A25	D10	X1-86	I/O, TS	Address Bus A25
A26	C10	X1-85	I/O, TS	Address Bus A26
A27	A13	X1-84	I/O, TS	Address Bus A27
A28	A10	X1-83	I/O, TS	Address Bus A28
A29	A12	X1-82	I/O, TS	Address Bus A29
A30	A11	X1-81	I/O, TS	Address Bus A30
A31	A9	X1-80	I/O, TS	Address Bus A31 (LSB)
PA0	U19	X2-28	I/O	Port PA0
PA1	T19	X2-29	I/O	Port PA1
PA2	R18	X2-30	I/O	Port PA2
PA3	P17	X2-31	I/O	Port PA3
PA4	P19	X2-32	I/O	Port PA4
PA5	N18	X2-33	I/O	Port PA5
PA6	M17	X2-34	I/O	Port PA6
PA7	M19	X2-35	I/O	Port PA7
PA8	L17	X2-36	I/O	Port PA8
PA9	K18	X2-37	I/O	Port PA9
PA10	J17	X2-38	I/O	Port PA10
PA11	G16	X2-39	I/O	Port PA11
PA12	F17	X2-40	I/O	Port PA12
PA13	E17	X2-41	I/O	Port PA13
PA14	D17	X2-42	I/O	Port PA14
PA15	C18	X2-43	I/O	Port PA15
PB14	U18	X2-48	I/O	Port PB14
PB15	R17	X2-49	I/O	Port PB15
PB16	N16	X2-50	I/O	Port PB16
PB17	P18	X2-51	I/O	Port PB17
PB18	N17	X2-52	I/O	Port PB18
PB19	N19	X2-53	I/O	Port PB19
PB20	L16	X2-54	I/O	Port PB20 used as SMRXD2#, connected to RS232-Driver TTL-Output via a 4k7 resistor for decoupling for other usage
PB21	K16	X2-55	I/O	Port PB21 used as SMTXD2#, connected to RS232-Driver TTL-Input
PB22	L19	X2-56	I/O	Port PB22
PB23	K17	X2-57	I/O	Port PB23
SMRXD1# RXD3# PB24	J18	X2-58	I/O	Port PB24 used as SMRXD1# or RXD3#, connected to RS232-Driver TTL-Output via a 4k7 resistor for decoupling for other usage
SMTXD1# TXD3# PB25	J16	X2-59	I/O	Port PB25 used as SMTXD1# or TXD3#, connected to RS232-Driver TTL-Input
PB26	F19	X2-60	I/O	Port PB26

Signal	CPU-Pin	Module-Pin	Type	Description TQM855L / TQM860L
PB27	E19	X2-61	I/O	Port PB27
PB28	D19	X2-62	I/O	Port PB28
PB29	E16	X2-63	I/O	Port PB29
PB30	C19	X2-64	I/O	Port PB30
PB31	C17	X2-65	I/O	Port PB31
PC4	T17	X2-16	I/O	Port PC4
PC5	T18	X2-17	I/O	Port PC5
PC6	R19	X2-18	I/O	Port PC6
PC7	M16	X2-19	I/O	Port PC7
PC8	M18	X2-20	I/O	Port PC8
PC9	L18	X2-21	I/O	Port PC9
PC10	K19	X2-22	I/O	Port PC10
PC11	J19	X2-23	I/O	Port PC11
PC12	F18	X2-24	I/O	Port PC12
PC13	E18	X2-25	I/O	Port PC13
PC14	D18	X2-26	I/O	Port PC14
PC15	D16	X2-27	I/O	Port PC15
PD3	W16	X2-03	I/O	Port PD3
PD4	U16	X2-04	I/O	Port PD4
PD5	U15	X2-05	I/O	Port PD5
PD6	V16	X2-06	I/O	Port PD6
PD7	T15	X2-07	I/O	Port PD7
PD8	W17	X2-08	I/O	Port PD8
PD9	V17	X2-09	I/O	Port PD9
PD10	W18	X2-10	I/O	Port PD10
PD11	T16	X2-11	I/O	Port PD11
PD12	R16	X2-12	I/O	Port PD12
PD13	V18	X2-13	I/O	Port PD13
PD14	V19	X2-14	I/O	Port PD14
PD15	U17	X2-15	I/O	Port PD15
IRQ0#	V14	X1-02	I	Interrupt Request 0, pull-up 4k7
IRQ1#	U14	X1-03	I	Interrupt Request 1, pull-up 4k7
IRQ2# RSV#	H3	X1-04	I/O, TS	Interrupt Request 2 / Reservation, pull-up 4k7
IRQ3#	V3	X1-05	I/O, TS	Interrupt Request 3, pull-up 4k7
IRQ_CAN# IRQ4#	V5	X1-06	I/O, TS	Interrupt Request 4 used as CAN Interrupt, connected to P2.6/INT# of both AS82527 devices, pull-up 4k7
IRQ5#	W4	X1-07	I/O, TS	Interrupt Request 5, pull-up 4k7
IRQ6#	V4	X1-08	I/O, TS	Interrupt Request 6, pull-up 4k7
IRQ7#	W15	X1-09	I	Interrupt Request 7, pull-up 4k7
CLKOUT	W3	X1-40	O	System Clock Output
EXTCLK	N2	X1-39	I	External Clock Input
TEXP	N3	X1-36	O	Timer Expired Output
PORESET#	R2	X1-35	O	Power-On Reset connected to Reset Device / Voltage Supervisor for 3,3 and 5 V
HRESET#	N4	X1-37	I/O, OD	Hard Reset, pull-up 1k0

Signal	CPU-Pin	Module-Pin	Type	Description TQM855L / TQM860L
SRESET#	P2	X1-42	I/O, OD	Soft Reset, pull-up 10k, drives Reset LED
RSTCONF#	P3	X1-38	I	Reset Configuration, Pull-Down 1k
DSDI/TDI	H17	X2-44	I	Development Serial Data Input / Test Data Input, Pull-Down 10k
DSDO/TDO	G17	X2-45	O, TS	Development Serial Data Output / Test Data Output
DSCK/TCK	H16	X2-46	I	Development Serial Clock / Test Clock, Pull-Down 10k
TMS	G18	X2-47	I	Test Mode Select, pull-up 10k
BS_A0#	D8	X1-56	O	Byte Select A0
BS_A1#	C8	X1-57	O	Byte Select A1
BS_A2#	A7	X1-58	O	Byte Select A2
BS_A3#	B8	X1-59	O	Byte Select A3
WE0# BS_B0#	C7	X1-76	O	Write Enable / Byte Select B0
WE1# BS_B1#	A6	X1-77	O	Write Enable / Byte Select B1
WE2# BS_B2#	B6	X1-78	O	Write Enable / Byte Select B2
WE3# BS_B3#	A5	X1-79	O	Write Enable / Byte Select B3
CS_FLASH0# CS0#	C3	X1-71	O	Chip Select 0 used as (Boot) FLASH Chip Select
CS_FLASH1# CS1#	A2	X1-70	O	Chip Select 1 used as FLASH Chip Select
CS2# CS_SDRAM0- #	D4	X1-69	O	Chip Select 2 used as SDRAM Chip Select
CS_CAN# CS3#	E4	X1-68	O	Chip Select 3 used as CAN Chip Select
CS4#	A4	X1-67	O	Chip Select 4
CS5#	B4	X1-66	O	Chip Select 5
CS6# CE_1B#	D5	X1-65	O	Chip Select 6 / Card Enable 1 Slot B
CS7# CE_2B#	C4	X1-64	O	Chip Select 7 / Card Enable 2 Slot B
CE1_A#	B3	X1-54	O	Card Enable 1 Slot A
CE2_A#	A3	X1-55	O	Card Enable 2 Slot A
RD/WR#	B2	X2-73	O	Read / Write RD/WR#
BB#	E1	X2-75	I/O	Bus Busy
BG#	E2	X2-74	I/O	Bus Grant, pull-up 2k2
BR#	G4	X2-76	I/O	Bus Request, pull-up 4k7
BURST#	F1	X2-82	I/O, TS	Burst Transaction
BI#	E3	X2-81	I/O, TS	Burst Inhibit, pull-up 4k7
BDIP# GPL_B5#	D2	X1-63	I/O, TS	Burst Data in Progress General Purpose Line B5
GPL_A5#	D3	X1-62	O	General Purpose Line A5 used for CAN
UPWAITB GPL_B4#	B1	X1-61	I/O	User Programmable Machine Wait B General Purpose Line B4
UPWAITA GPL_A4	C1	X1-60	I/O	User Programmable Machine Wait A General Purpose Line A4 used for CAN
GPL_AB3#	C5	X1-75	O	General Purpose Line A3 / B3 used for SDRAM
GPL_AB2#	B5	X1-74	O	General Purpose Line A2 / B2 used for SDRAM and CAN

Signal	CPU-Pin	Module-Pin	Type	Description TQM855L / TQM860L
OE# GPL_AB1#	C6	X1-73	O	Output Enable General Purpose Line A1 / B1 used for SDRAM and FLASH
GPL_AB0#	D7	X1-72	O	General Purpose Line A0 / B0
WAIT_A#	R3	X1-10	I	Wait Slot A, pull-up 4k7
ALE_A	K2	X1-11	I/O, TS	Address Latch Enable Slot A ***??? only Output
IPA0	T5	X1-12	I	Input Port A0
IPA1	T4	X1-13	I	Input Port A1
IPA2	U3	X1-14	I	Input Port A2
IPA3	W2	X1-15	I	Input Port A3
IPA4	U4	X1-16	I	Input Port A4
IPA5	U5	X1-17	I	Input Port A5
IPA6	T6	X1-18	I	Input Port A6
IPA7	T3	X1-19	I	Input Port A7
WAIT_B#	R4	X1-24	I	Wait Slot B, pull-up 4k7
ALE_B	J1	X1-25	I/O, TS	Address Latch Enable Slot B
IPB0	H2	X1-33	I	Input Port B0
IPB1	J3	X1-32	I	Input Port B1
IPB2	J2	X1-31	I	Input Port B2
IPB3	G1	X1-30	I	Input Port B3
IPB4	G2	X1-29	I	Input Port B4
IPB5	J4	X1-28	I	Input Port B5
IPB6	K3	X1-27	I	Input Port B6
IPB7	H1	X1-26	I	Input Port B7
OP0	L4	X1-21	O	Output Port 0
OP1	L2	X1-20	O	Output Port 1
MODCK1 OP2	L1	X1-22	I/O	Mode Clock 1 Output Port 2
MODCK2 OP3	M4	X1-23	I/O	Mode Clock 2 Output Port 3
TS#	F3	X2-83	I/O, TS	Transfer Start, pull-up 4k7
TA#	C2	X2-77	I/O, TS	Transfer Acknowledge, pull-up 2k2
TEA#	D1	X2-80	I/O, OD	Transfer Error Acknowledge, pull-up 2k2
TSIZ0 REG#	B9	X2-78	I/O, TS	Transfer Size 0 / Register
TSIZ1	C9	X2-79	I/O, TS	Transfer Size 1
IRQ4# KR# RETRY	K1	X2-72	I/O	Interrupt Request 4 / Kill Reservation / Retry
CR# IRQ3#	F2	X2-70	I	Cancel Reservation / Interrupt Request 3
FRZ IRQ6#	G3	X2-71	I/O	Freeze / Interrupt Request 6
AS#	L3	X2-69	I	Address Strobe
BADDR28	M3	X2-68	O	Burst Address 28
BADDR29	M2	X2-67	O	Burst Address 29
BADDR30 REG#	K4	X2-66	O	Burst Address 30 / Register
Spare1	B7	X2-87	-	Spare1
Spare2	H18	X2-86	-	Spare2
Spare3	V15	X2-85	-	Spare3
Spare4	H4	X2-84	-	Spare4

5.6.4 Non-CPU Pins for TQM855L / TQM860

Signal	Type	Module-Pin	Description TQM855L / TQM860
VCC3V3	-	X1-112	3.3 V Supply
VCC3V3	-	X1-113	3.3 V Supply
VCC3V3	-	X1-114	3.3 V Supply
VCC5V	-	X1-116	5 V Supply
VCC5V	-	X1-118	5 V Supply
VCC5V	-	X1-120	5 V Supply
VBAT	-	X2-01	Battery Input, connected to KAPWR via Schottky Diode
DGND	-	X1-115	Digital Ground
DGND	-	X1-117	Digital Ground
DGND	-	X1-119	Digital Ground
DGND	-	X1-01	Digital Ground
DGND	-	X2-02	Digital Ground
DGND	-	X2-120	Digital Ground
SMRXD1	I	X1-52	SMRXD1# via RS232 receiver
SMTXD1	O	X1-53	SMTXD1# via RS232 driver
SMRXD2	I	X1-50	SMRXD2# via RS232 receiver
SMTXD2	O	X1-51	SMTXD2# via RS232 driver
RX0-CAN1	I	X1-49	Single-Ended CAN Receive 1
TX0-CAN1	O	X1-48	Single-Ended CAN Transmit 1
RX0-CAN2	I	X1-47	Single-Ended CAN Receive 2
TX0-CAN2	O	X1-46	Single-Ended CAN Transmit 2
ENMON#	I	X1-41	Enable Monitor. Pull low to enable MON8xx after Reset. Must be stable for min. 50 ms after PORESET becomes inactive. pull-up 10k.
JTAG/BDM#	I	X1-43	JTAG / BDM Select. Pull low to enable BDM. pull-up 10k.
HRESETF#	I	X1-44	Hard Reset at FLASH. Can be used to connect 12 V to FLASHes' RESET pin without damage to the module.
CKE	I	X1-45	Clock Enable of SDRAMs. May be pulled low to enter SDRAM Power Down. pull-up 4k7.
RESIN#	I	X1-34	Reset Input. Connected to Reset device. pull-up 4k7.

6 Power Supply

This chapter describes the TQM8xxL power supply.

6.1 Power Supply 3.3V

Most of the module's components, including the CPU, use a 3.3 V supply. The 3.3 V may either be generated by the on-board DC/DC-converter, or provided by an external circuit. The requirements are:

Voltage	3.17 .. 3.6 V	Determined by components' ratings and voltage supervisor threshold
Ripple	40 mV	Peak to peak
Converter output current	670 mA	Worst case value (min.)
Module supply current	670 mA	Worst case value (max.)
External supply current	0	No current may be drawn externally

6.2 Power Supply 5V

On the TQM8xxL, only the CAN circuitry uses a 5 V supply.

Voltage	4,5 .. 5,5 V	Determined by components' ratings and voltage supervisor threshold
Ripple	60 mV	Peak to peak
Module supply current	150 mA	Worst case value (max.)

6.3 Battery Input

The TQM8xxL uses VBAT only for the CPU's KAPWR (Keep Alive Power), which supplies the on-chip RTC. VBAT will only be loaded when VCC3V3 is down.

Voltage	2.0 .. 3,6 V	Lower threshold is not yet specified by Motorola
Module supply current	20 mA* 10 µA	Worst case value (max.)

* Value for MPC mask sets with RTC bug, i. e. MPC860 including C1 mask, MPC850 and MPC823 including 0.1 mask

7 ESD

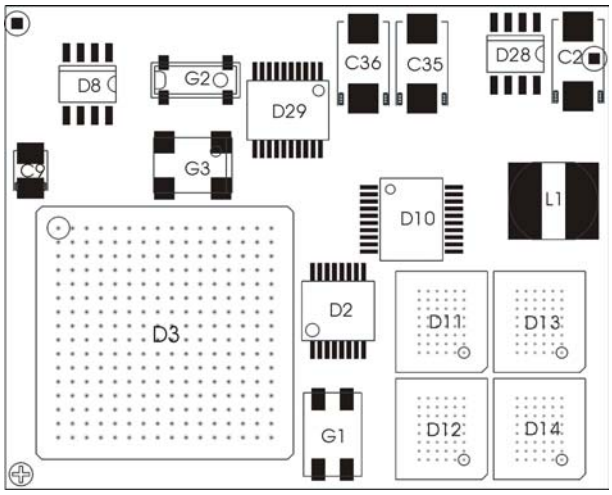
You need to use precautions to avoid electrostatic discharge (ESD) damage to the TQ Minimodules.
TQ Minimodule are designed due to the EMI requirement. Most I/O Lines of the Minimodul are connected direct from Processor Pin to the header, so the TQ Minimodules should not be operated without protection circuitry on the Target platform.

8 Technical Data

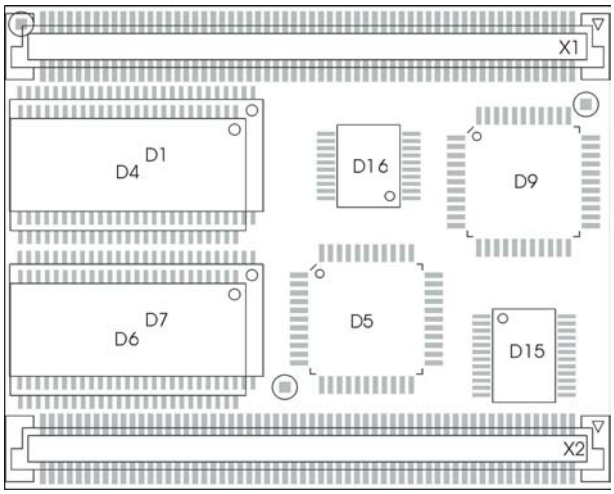
PCB-Material:	FR4
PCB-Layout:	double sided SMT
PCB-Layer:	8 Layer including 2 Microvia
Dimension:	81,6 x 54 mm²
Ambient Operating Temperature:	0°C - 70°C
Optional Operating Temperature:	-40°C - +85°C
Storage Temperature Range:	-20°C - +85°C
Power Supply:	see 6.1 / 6.2
Power Dissipation	Worst case 2,7W

8.1 View

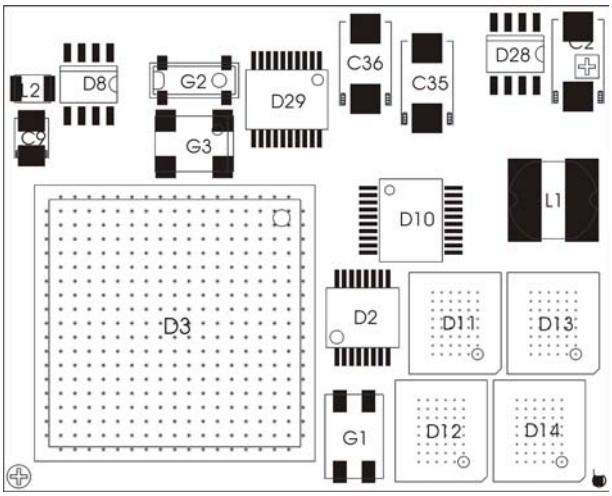
TQM823L/850L Top-View



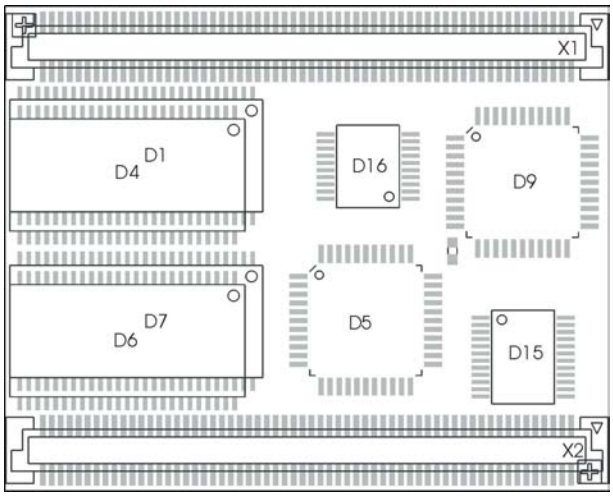
TQM823L/850L Bottom-View



TQM855L/860L Top-View



TQM855L/860L Bottom-View



9 Mechanical Data and Pin Configuration

9.1 Connector

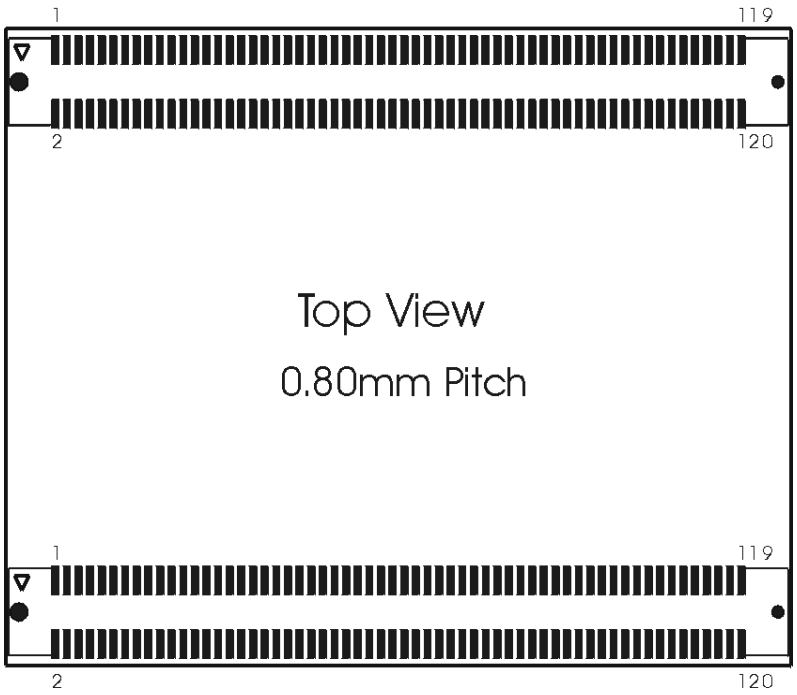
9.1.1 Connector Reference No.

The Board to Board Connector which are used for the Minimodules are high reliable Connector with 0.8 mm Pitch. For the Minimodule following Connectors are used:

Board-to-Board Distance	No.	Module				Baseboard
		No. of Pin	Qty.	Manufacturer	No.	No.
5 mm	A	120	2	AMP Berg	177983-5 61082-121000	177984-5 61083-121000
6 mm						179029-5 61083-122000
7 mm						179030-5 61083-123000
8 mm						179031-5 61083-124000

9.1.2 Connector Location

TQM8xxL Topview



9.2 Pin Configuration

Connector X1					
Pin No.	TQM823L/850L	TQM855L/860L	Pin No.	TQM823L/850L	TQM855L/860L
2	IRQ0#	IRQ0#	1	DGND	DGND
4	IRQ2#/RSV#	IRQ2#/RSV#	3	IRQ1#	IRQ1#
6	IRQ4# IRQ_CAN#	IRQ4# IRQ_CAN#	5	IRQ3#	IRQ3#
8	IRQ6#	IRQ6#	7	IRQ5#	IRQ5#
10	NC	WAIT_A#	9	IRQ7#	IRQ7#
12	NC	IP_A0	11	NC	ALE_A
14	NC	IP_A2	13	NC	IP_A1
16	NC	IP_A4	15	NC	IP_A3
18	NC	IP_A6	17	NC	IP_A5
20	NC	OP1	19	NC	IP_A7
22	OP2/MODCK1	OP2/MODCK1	21	NC	OP0
24	WAIT_B#	WAIT_B#	23	OP3/MODCK2	OP3/MODCK2
26	IP_B7	IP_B7	25	ALE_B	ALE_B
28	IP_B5	IP_B5	27	IP_B6	IP_B6
30	IP_B3	IP_B3	29	IP_B4	IP_B4
32	IP_B1	IP_B1	31	IP_B2	IP_B2
34	RESIN#	RESIN#	33	IP_B0	IP_B0
36	TEXP	TEXP	35	PORESET#	PORESET#
38	RSTCONF#	RSTCONF#	37	HRESET#	HRESET#
40	CLKOUT	CLKOUT	39	EXTCLK	EXTCLK
42	SRESET#	SRESET#	41	ENMON#	ENMON#
44	HRESETF#	HRESETF#	43	JTAG/BDM#	JTAG/BDM#
46	Tx0_CAN2	Tx0_CAN2	45	CKE	CKE
48	Tx0_CAN1	Tx0_CAN1	47	Rx0_CAN2	Rx0_CAN2
50	SMRxD2	SMRxD2	49	Rx0_CAN1	Rx0_CAN1
52	SMRxD1	SMRxD1	51	SMTxD2	SMTxD2
54	NC	CE_A1#	53	SMTxD1	SMTxD1
56	NC	BS_A0#	55	NC	CE2_A#
58	NC	BS_A2#	57	NC	BA_A1#
60	UPWAITA GPL_A4#	UPWAITA GPL_A4#	59	NC	BS_A3#

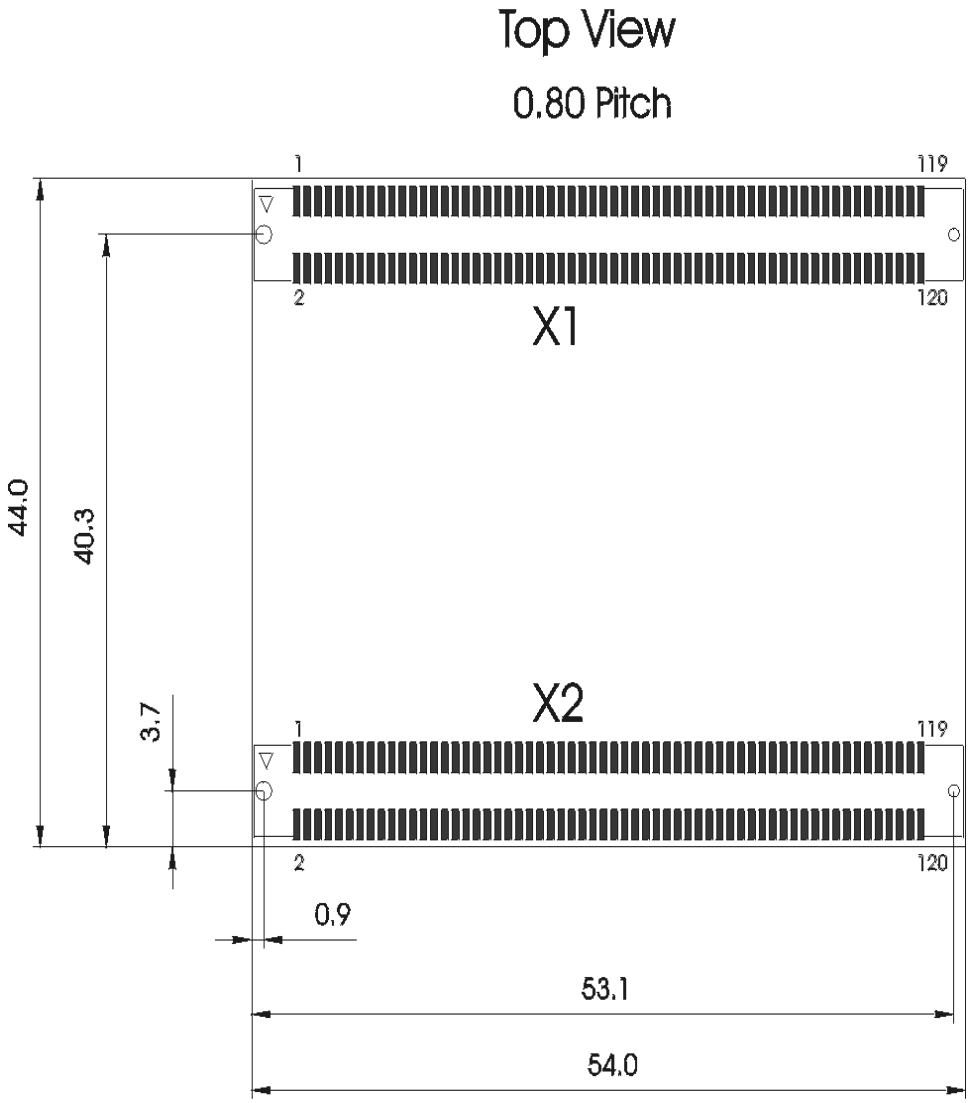
Connector X1					
Pin No.	TQM823L/850L	TQM855L/860L	Pin No.	TQM823L/850L	TQM855L/860L
62	GPL_A5#	GPL_A5#	61	UPWAITB GPL_B4#	UPWAITB GPL_B4#
64	CS7#/CE_2B#	CS7#/CE_2B#	63	BDIP#/GPL_B-5#	BDIP#/GPL_B5#
66	CS5#	CS5#	65	CS6#/CE_1B#	CS6#/CE_1B#
68	CS_CAN#/CS3#	CS_CAN#/CS3#	67	CS#4	CS#4
70	CS_FLASH1 CS1#	CS_FLASH1# CS1#	69	CS_SDRAM0 #CS2#	CS_SDRAM0 #CS2#
72	GP_AB0#	GP_AB0#	71	CS_FLASH0# CS0#	CS_FLASH0# CS0#
74	GPL_AB2#	GPL_AB2#	73	OE#/GPL_AB1-#	OE#/GPL_AB1#
76	WE0#/BS_AB0#	WE0#/BS_AB0#	75	GPL_AB3#	GPL_AB3#
78	WE2#/BS_AB2#	WE2#/BS_AB2#	77	WE1#/BS_AB-1#	WE1#/BS_AB1#
80	A31	A31	79	WE3#/BS_AB-3#	WE3#/BS_AB3#
82	A29	A29	81	A30	A30
84	A27	A27	83	A28	A28
86	A25	A25	85	A26	A26
90	A21	A21	89	A22	A22
92	A19	A19	91	A20	A20
94	A17	A17	93	A18	A18
96	A15	A15	95	A16	A16
98	A13	A13	97	A14	A14
100	A11	A11	99	A12	A12
102	A9	A9	101	A10	A10
104	A7	A7	103	A8	A8
106	NC	A5	105	A6	A6
108	NC	A3	107	NC	A4
110	NC	A1	109	NC	A2
112	VCC3V3	VCC3V3	111	NC	A0
114	VCC3V3	VCC3V3	113	VCC3V3	VCC3V3
116	VCC5V	VCC5V	115	DGND	DGND
118	VCC5V	VCC5V	117	DGND	DGND
120	VCC5V	VCC5V	119	DGND	DGND

Connector X2					
Pin No.	TQM823L/850L	TQM855L/860L	Pin No.	TQM823L/85-0L	TQM855L/860L
2	DGND	DGND	1	VBAT	VBAT
4	PD4	PD4	3	PD3	PD3
6	PD6	PD6	5	PD5	PD5
8	PD8	PD8	7	PD7	PD7
10	PD10	PD10	9	PD9	PD9
12	PD12	PD12	11	PD11	PD11
14	PD14	PD14	13	PD13	PD13
16	PC4	PC4	15	PD15	PD15
18	PC6	PC6	17	PC5	PC5
20	PC8	PC8	19	PC7	PC7
22	PC10	PC10	21	PC9	PC9
24	PC12	PC12	23	PC11	PC11
26	PC14	PC14	25	PC13	PC13
28	NC	PA0	27	PC15	PC15
30	NC	PA2	29	NC	PA1
32	PA4	PA4	31	NC	PA3
34	PA6	PA6	33	PA5	PA5
36	PA8/SMTxD2#	PA8	35	PA7	PA7
38	NC	PA10	37	PA9/SMRxD-2#	PA9
40	PA12	PA12	39	NC	PA11
42	PA14	PA14	41	PA13	PA13
44	DSDI/TDI	DSDI/TDI	43	PA15	PA15
46	DSCK/TCK	DSCK/TCK	45	DSDO/TDO	DSDO/TDO
48	NC	PB14	47	TMS	TMS
50	PB16	PB16	49	NC	PB15
52	PB18	PB18	51	PB17	PB17
54	NC	PB20/SMRxD2#	53	PB19	PB19
56	PB22	PB22	55	NC	PB21/SMTxD2#
58	PB24/SMRxD1#	PB24/SMRxD1#	57	PB23	PB23
60	PB26	PB26	59	PB25/SMTxD-1	PB25/SMTxD1#

Connector X2					
Pin No.	TQM823L/850L	TQM855L/860L	Pin No.	TQM823L/850L	TQM855L/860L
62	PB28	PB28	61	PB27	PB27
64	PB30	PB30	63	PB29	PB29
66	NC	BADDR30/REG-#	65	PB31	PB31
68	NC	BADDR28	67	NC	BADDR29
70	NC	CR#/IRQ3#	69	NC	AS#
72	KR# IRQ4#/RETRY	KR# IRQ4#/RETRY	71	FRZ/IRQ6#	FRZ/IRQ6#
74	BG#	BG#	73	RD / WR#	RD / WR#
76	BR#	BR#	75	BB#	BB#
78	TSIZ0/REG#	TSIZ0/REG#	77	TA#	TA#
80	TEA#	TEA#	79	TSIZ1	TSIZ1
82	BURST#	BURST#	81	B#	B#
84	NC	SPARE4	83	TS#	TS#
86	SPARE2	SPARE2	85	SPARE3	SPARE3
88	D0	D0	87	NC	SPARE1
90	D2	D2	89	D1	D1
92	D4	D4	91	D3	D3
94	D6	D6	93	D5	D5
96	D8	D8	95	D7	D7
98	D10	D10	97	D9	D9
100	D12	D12	99	D11	D11
102	D14	D14	101	D13	D13
104	D16	D16	103	D15	D15
106	D18	D18	105	D17	D17
108	D20	D20	107	D19	D19
110	D22	D22	109	D21	D21
112	D24	D24	111	D23	D23
114	D26	D26	113	D25	D25
116	D28	D28	115	D27	D27
118	D30	D30	117	D29	D29
120	DGND	DGND	119	D31	D31

9.3 Mechanical Drawing

TQM8xxL Topview



9 Model No. and Order Code

TQM8 v v L w x y A z - t f

f: Frequenz
- 50 = 50Mhz
- 80 = 80Mhz

t: Processor Derivat
- E = MPC823e
- Blank = MPC823
- DE = MPC850DE
- SR = MPC850SR
- Blank = MPC850
- T = MPC855T
- DE = MPC860DE
- EN = MPC860EN
- SR = MPC860SR
- DT = MPC860DT
- T = MPC860T
- DP = MPC860DP
- P = MPC860P

z: Options
- 3 = Standard
- 2 = without DC/DC Converter

y: CAN Options
- 0 = no CAN Interface (Standard)
- B = with CAN1 / CAN2 Interface

x: SDRAM
- B = 16MByte (Standard)
- C = 32MByte
- D = 64MByte

w: FLASH
- C = 4MByte (Standard)
- D = 8MByte

vv: Processor Family
- 23 = MPC823
- 50 = MPC850
- 55 = MPC855
- 60 = MPC860

Valid Combinations

Not all Combinations will be in Mass Production. Consult TQ Components sales office to confirm availability of specific valid combinations and to check on newly released combinations.

10 References

Motorola:
http://www.mot.com/netcomm/docs/pubs/850UMAD_r0.pdf
http://www.mot.com/netcomm/aesop/mpc8XX/850/850_spec_workingfm.pdf
http://www.mot.com/netcomm/aesop/mpc8XX/850/mpc850errata.pdf
http://www.mot.com/netcomm/aesop/mpc8XX/860/deslist.pdf
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Author: *Zöpf 20.12.2000*

Release: *Heifi, 21.12.00*

TQ-Components GmbH * * Gut Delling, Mühlstr. 2 * D-82229 Seefeld i. OB / Germany
Tel: +49 8153/9308-0 * FAX: +49 8153/9308-134 * http://www.tqc.de * Email: support@tqc.de